Core Models

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Outline

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- ZSim core simulation techniques

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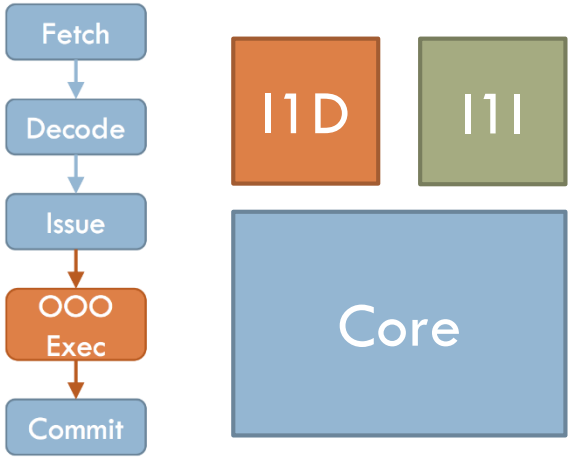
- ZSim core structure
  - Simple IPC 1 core
  - Timing core
  - OOO core



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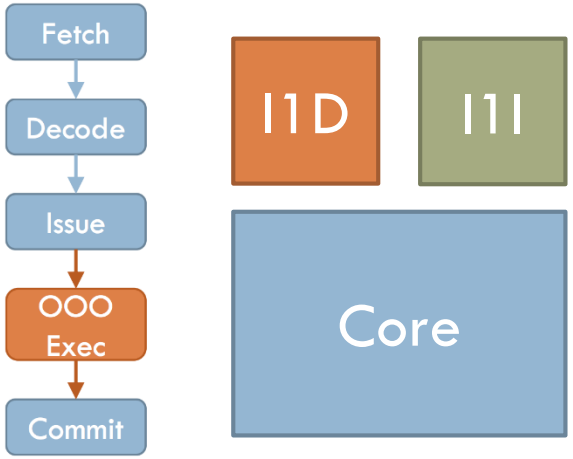

- Coding examples with demo
  - Branch predictor
  - Westmere to Silvermont

```
class GShareBranchPredictor {
    private:
        bool lastSeen;
    public:
        GShareBranchPredictor(){ lastSeen = false;}
        inline bool predict(Address branchPc, bool taken){
            bool prediction = (taken == lastSeen);
            lastSeen = taken;
            return prediction;
        }
};
```

Core Simulation Techniques

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- ZSim mainly uses 4 types of analysis routine
  - Basic block
  - Load and Store
  - Branch

  to cover the simulated program

Core Simulation Technique

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- A basic block (BBL) from Pin

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BblDescriptor:

numInstructions = 4

numBytes = 4

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```

Decode BBL into BBL descriptor

BblDescriptor:
numInstructions = 4
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uop[]

Core Simulation Technique

- Decode x86 instructions into uops
  - With different latencies, src/dst pair, function unit ports

Type	Src1	Src2	Dst1	Dst2	Lat	PortMsk
Load	rbp		rcx			001000
Exec	rbp		rdx		3	110001
Exec	rax	rdx	rdx	rflgs	1	110001
StAddr	rbp		S0		1	000100
StData	rdx	S0				000010
Exec	rax	rip	rip	rflgs	1	000001

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- 2. Simulate memory system operations with addresses

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mov (%rbp),%rcx
Load(%rbp)
add %rax,%rbx
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Store(%rbp)
BasicBlock(BblDescriptor)
ja 40530a
```

```
Load(Address addr) {
        L1D->load(addr);
}

Store(Address addr) {
        L1D->Store(addr);
}
```

Core Simulation Technique

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- Instruction-driven core activity (basic block) simulation
  - Simulates multiple stages for single instruction at once
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BasicBlock(BblDescriptor) {
        foreach uop {
                simulateFetch(uop);
                simulateDecode(uop);
                simulateIssue(uop);
                simulateExecute(uop);
                simulateCommit(uop);
        }
}
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                simulateIssue(uop);
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        }
}
```

```
simulateIssue(uop) {
    addUopToRob(curRobCycle, uop);
    if(rob.isFull()){
        nextRobAvailCycle = rob.advance();
    }
}
```

Core Simulation Technique

- Event-driven uncore activity simulation

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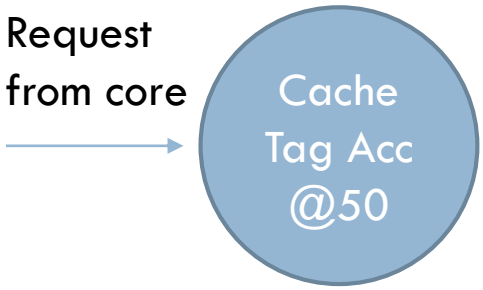
Request
from core

Core Simulation Technique

- Event-driven uncore activity simulation



Core Simulation Technique

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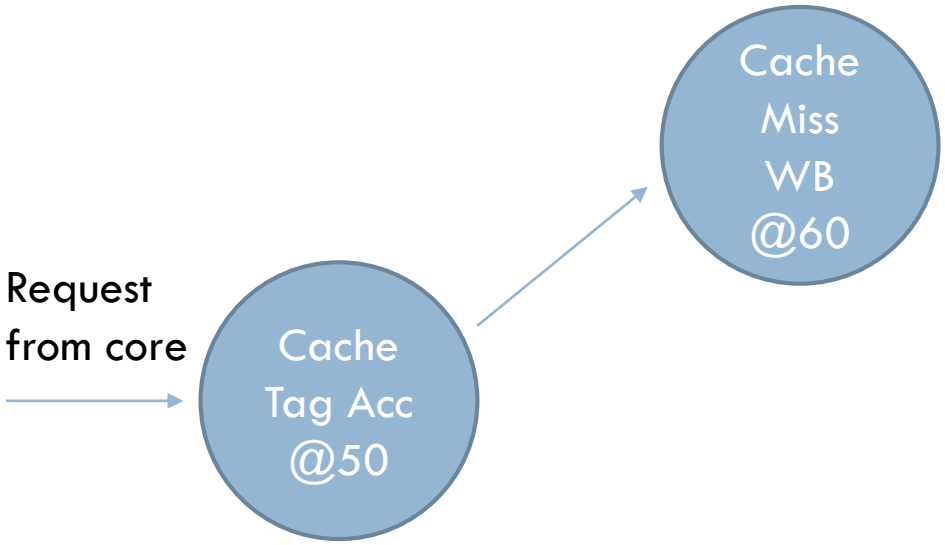

Core Simulation Technique

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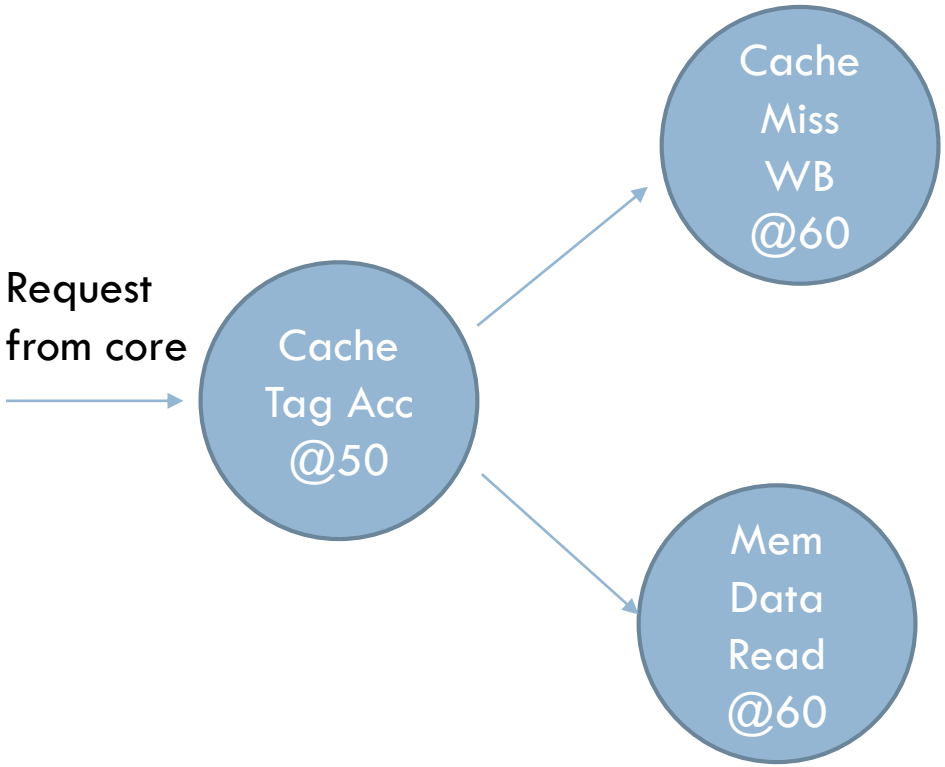

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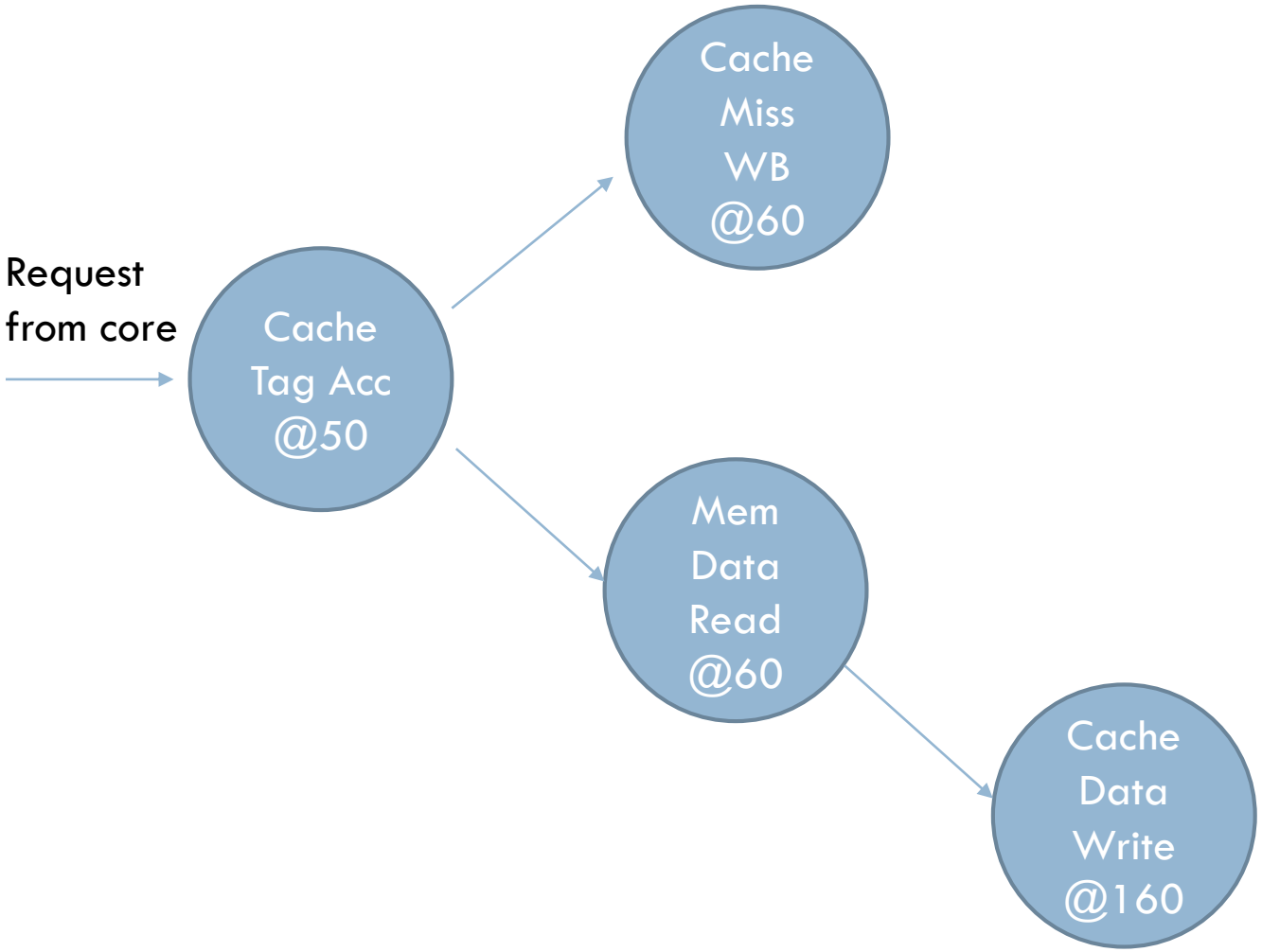

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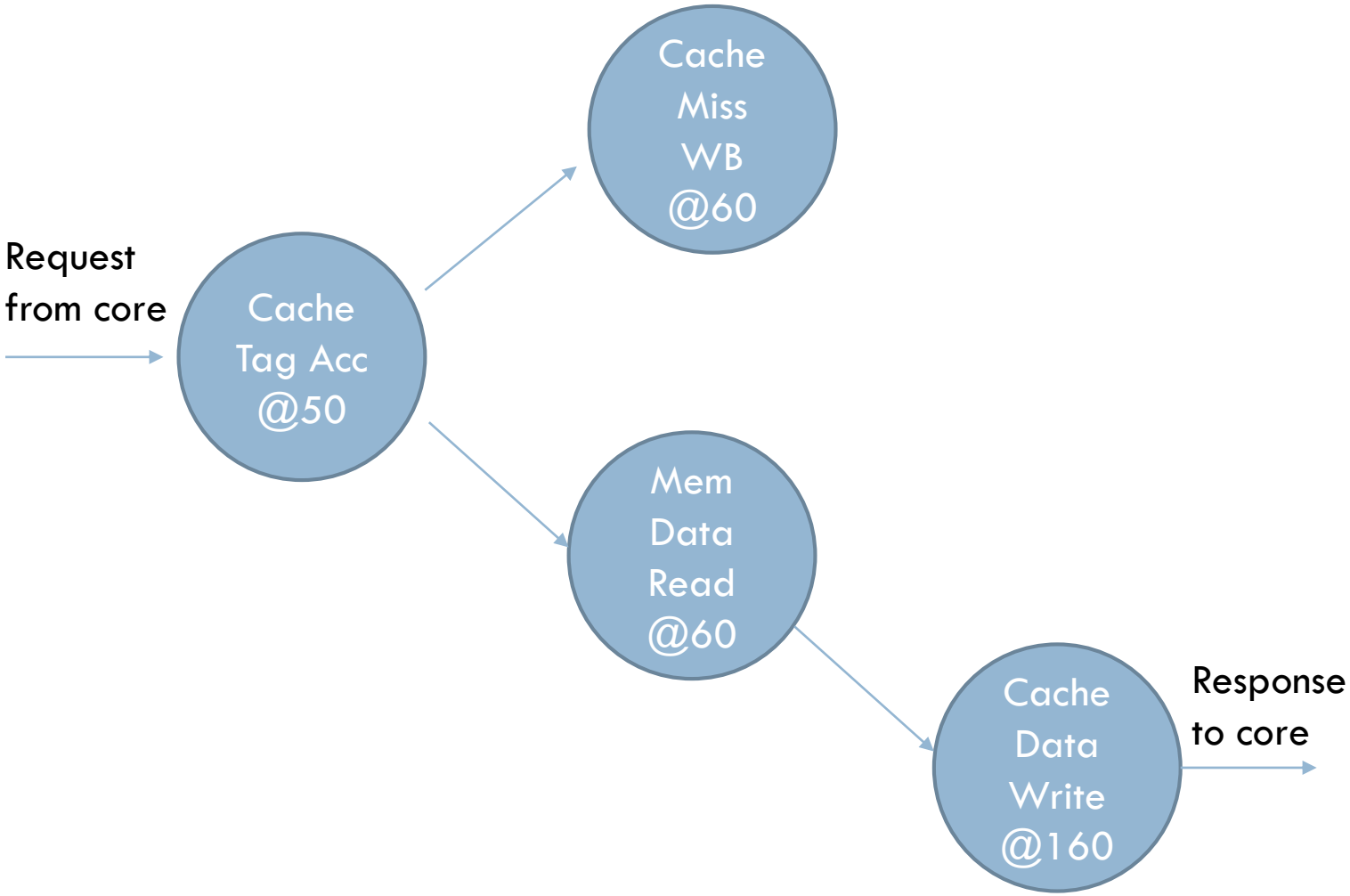

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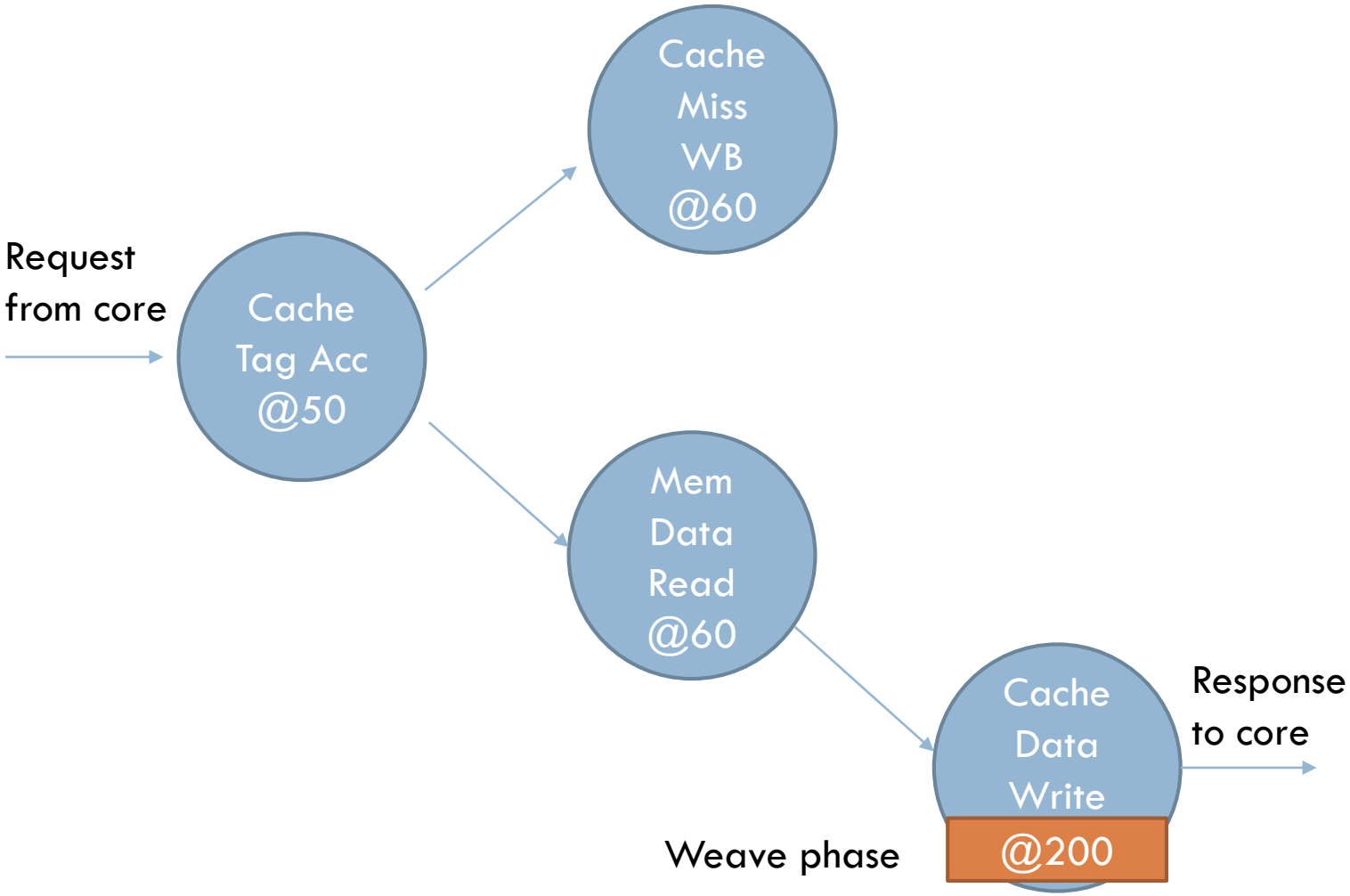

General Core Structure

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- ZSim simulates a core with 4 functions using Pin's APIs
  - BblFunc
  - LoadFunc
  - StoreFunc
  - BranchFunc

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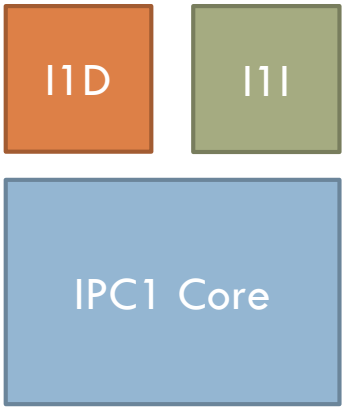
- ZSim simulates a core with 4 functions using Pin's APIs
  - BblFunc
  - LoadFunc
  - StoreFunc
  - BranchFunc
- Current supported core type
  - Simple IPC1 core
  - Timing core
  - OOO core (Westmere-like)

Simple IPC1 Core



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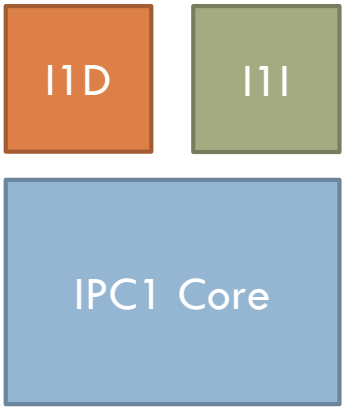

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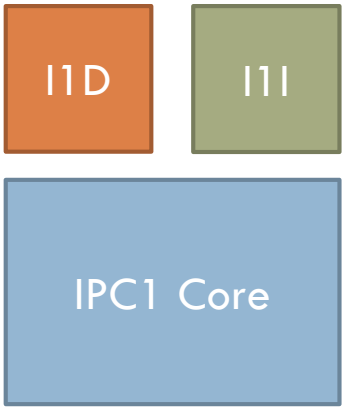

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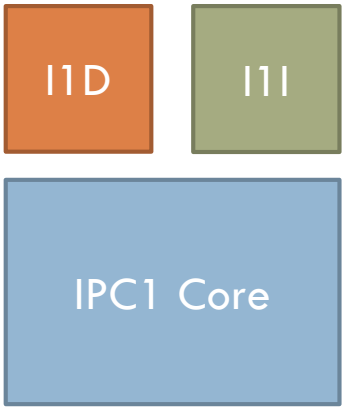

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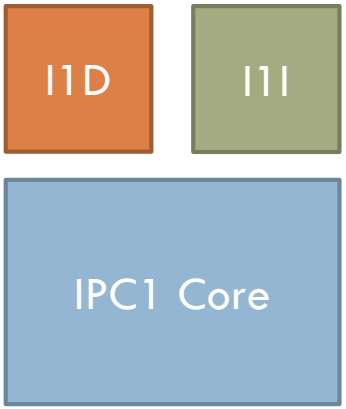

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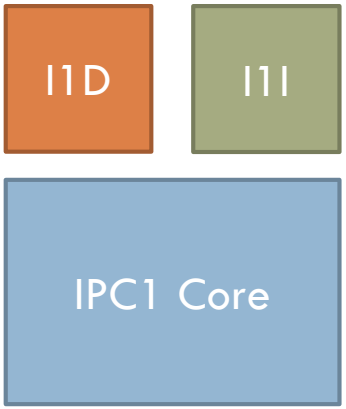

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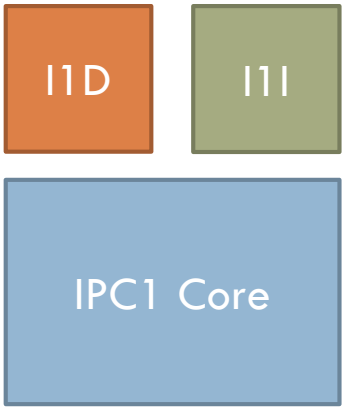

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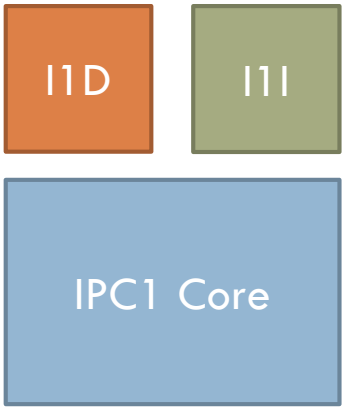
Current cycle += 4

Timing Core



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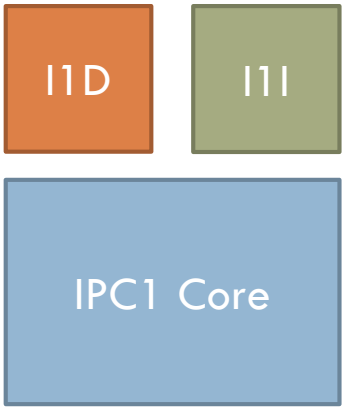

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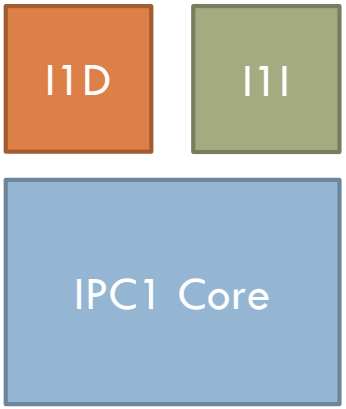

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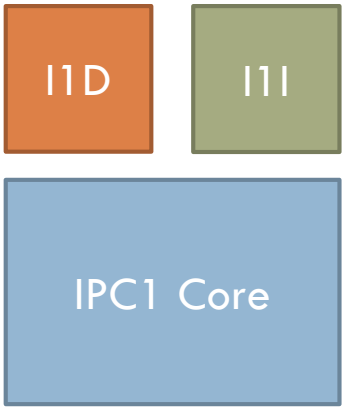

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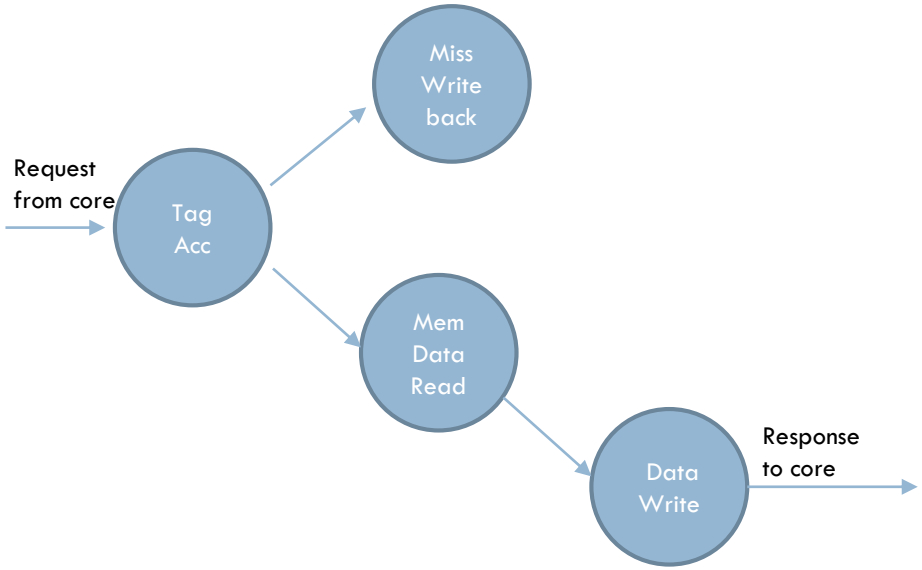

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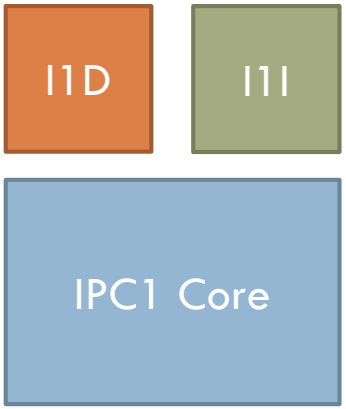

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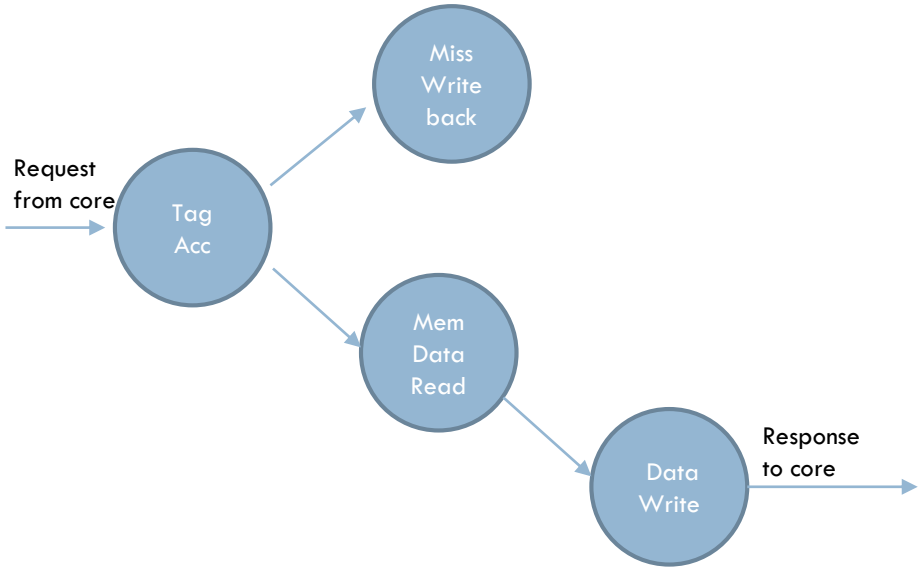

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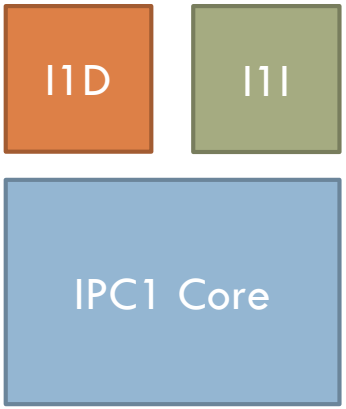

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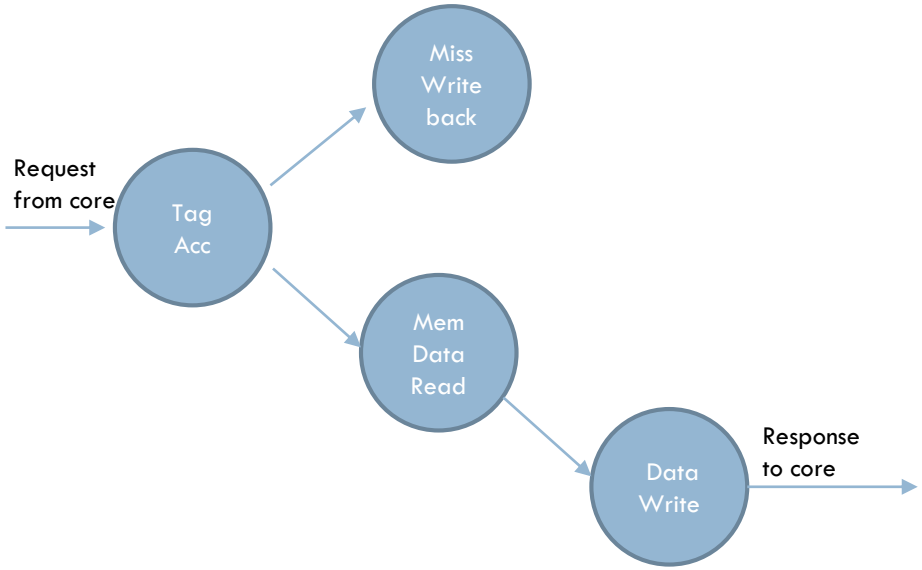

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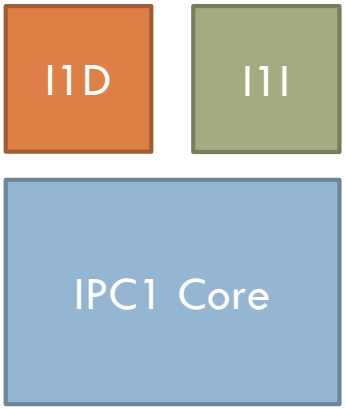

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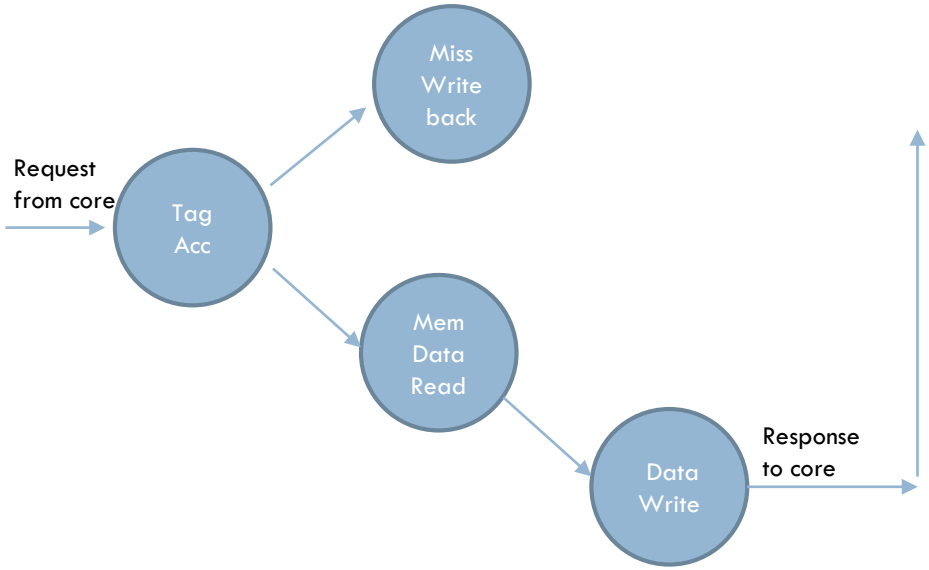

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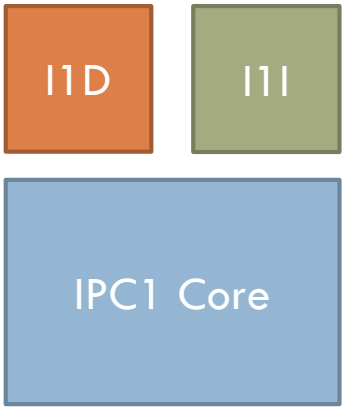

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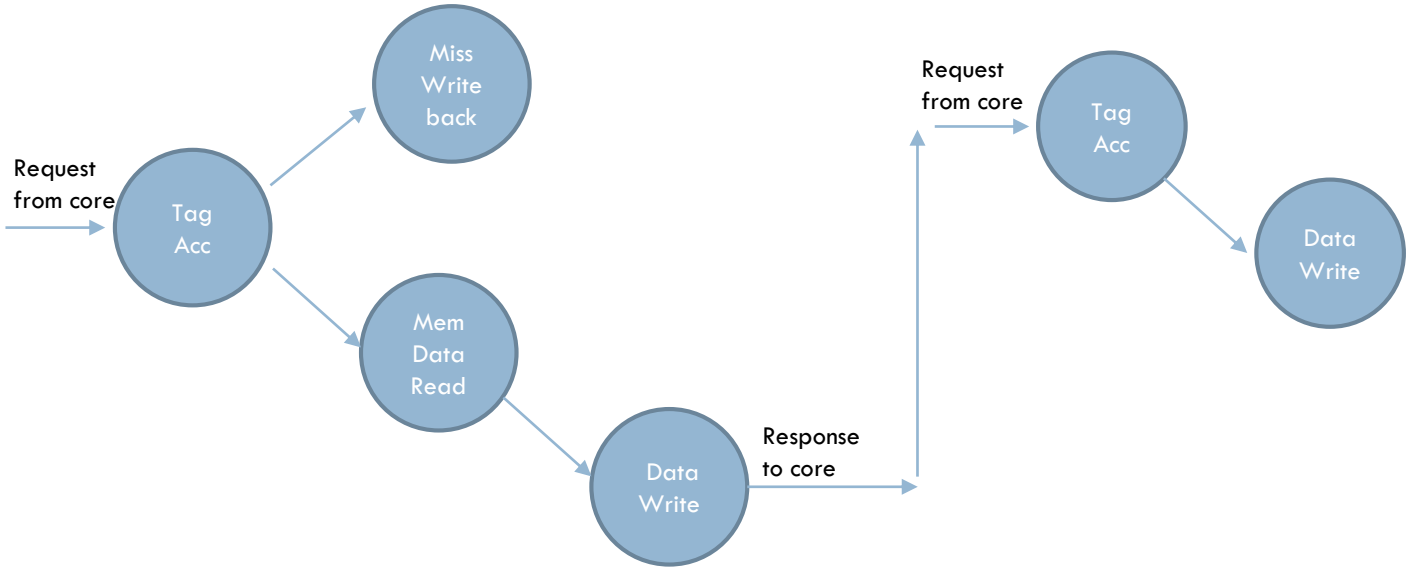

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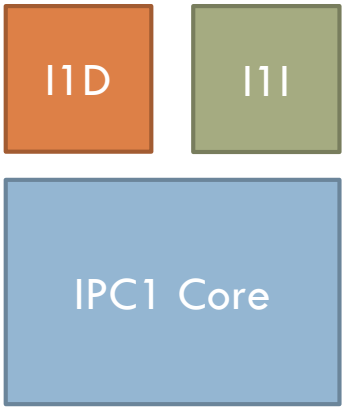

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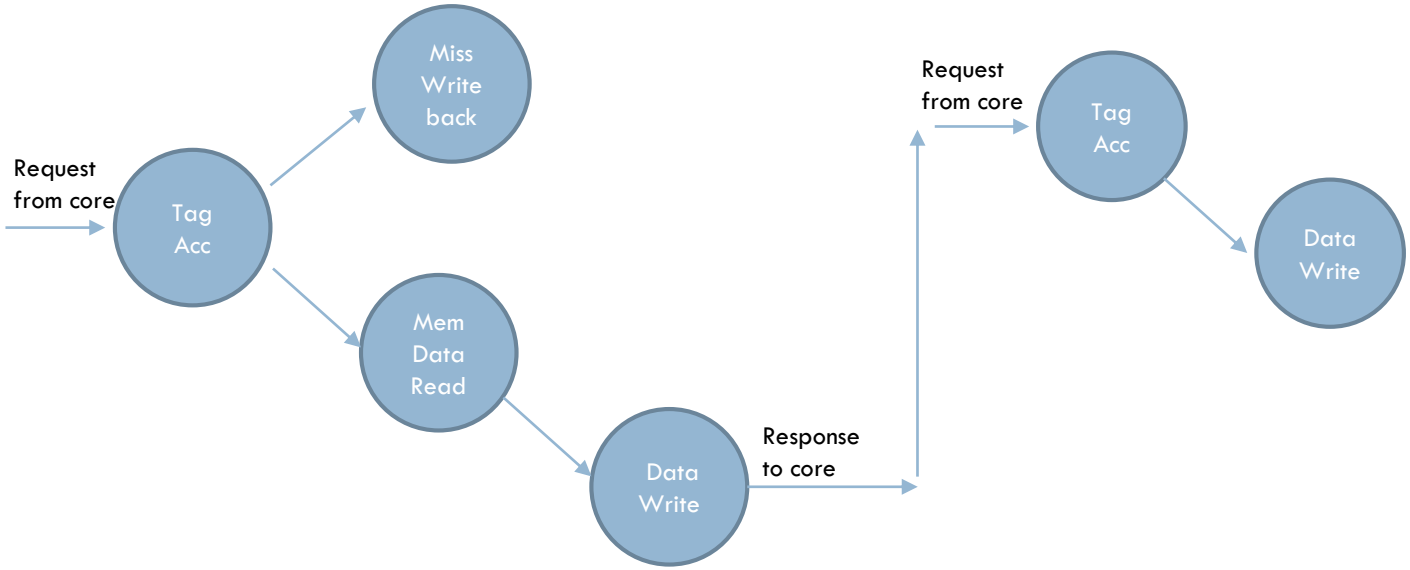

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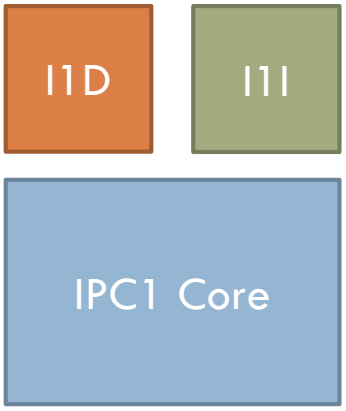

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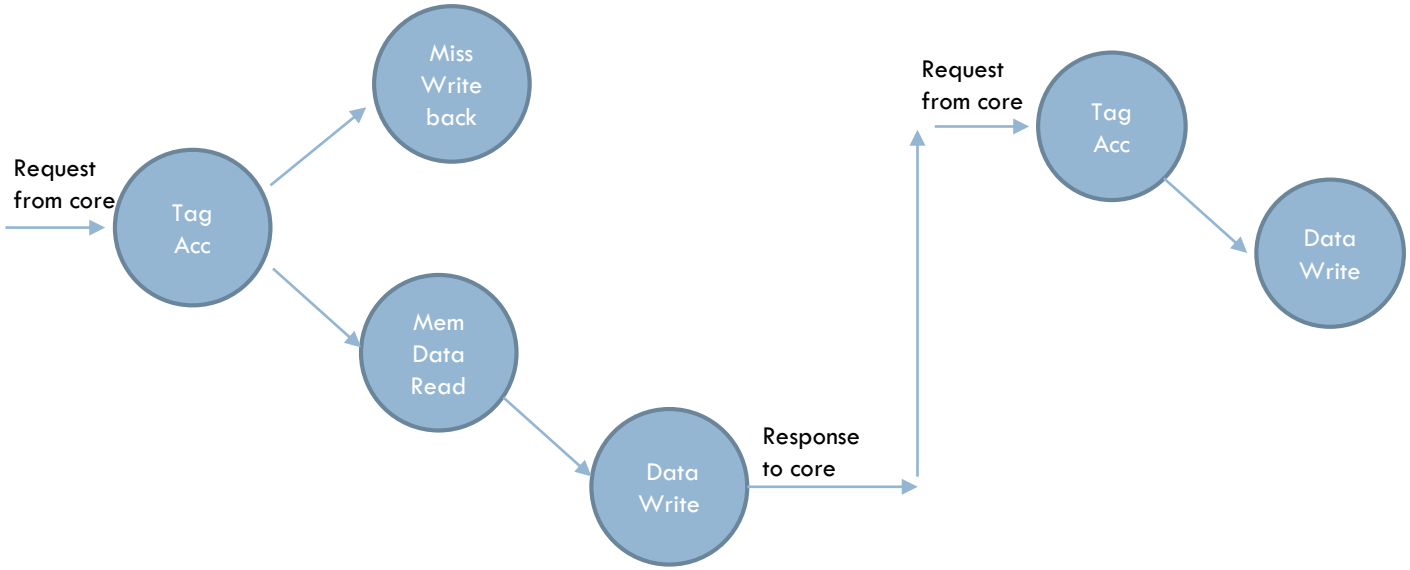
Current cycle += 4



OOO Core - BBL

- Simulate all stages at once

  Load A
  Exec
  Store A
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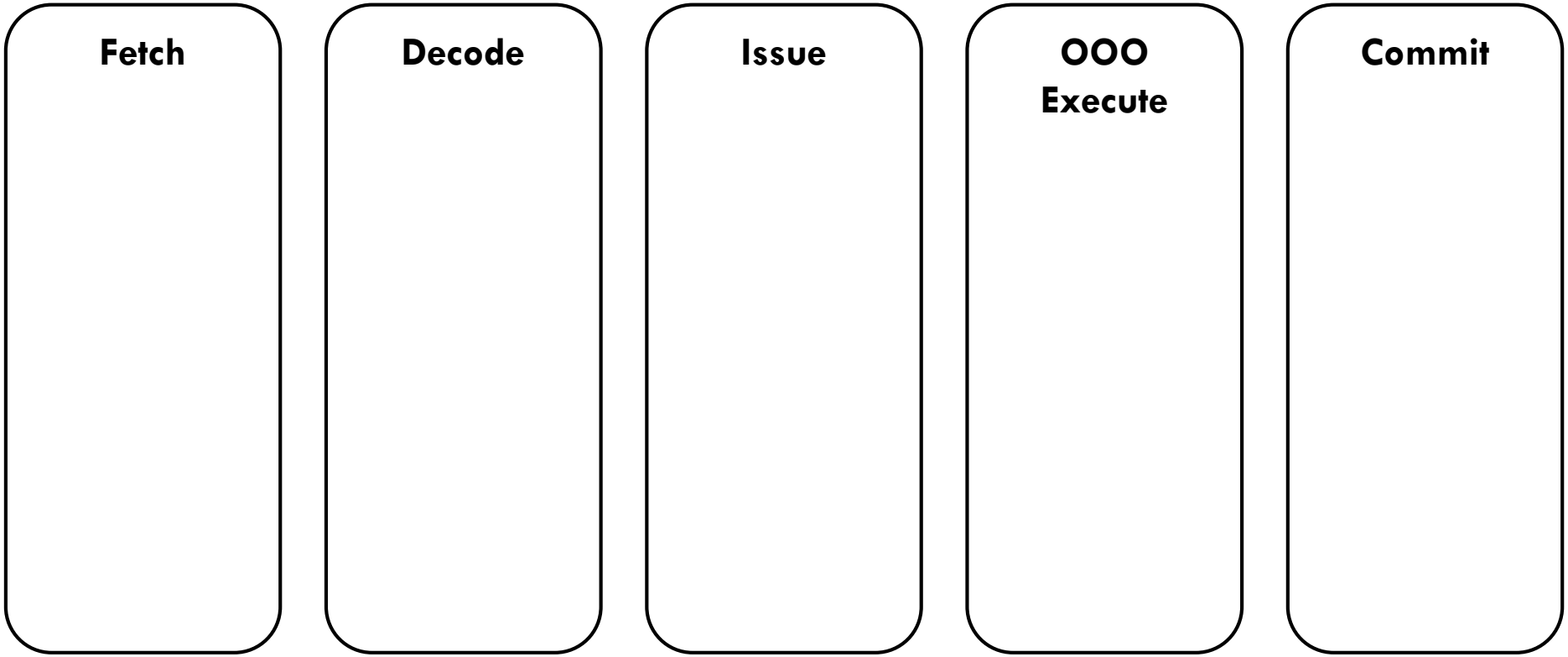

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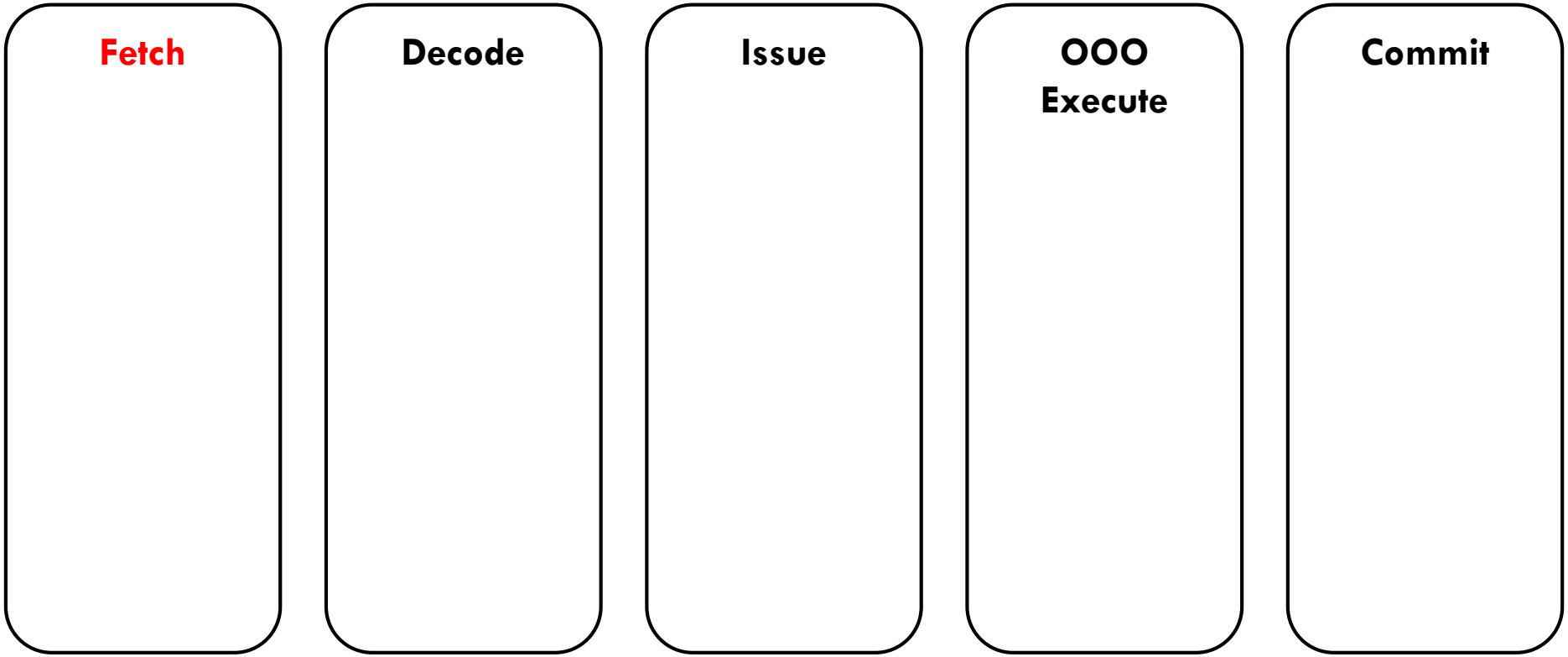

OOO Core - BBL

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Load A
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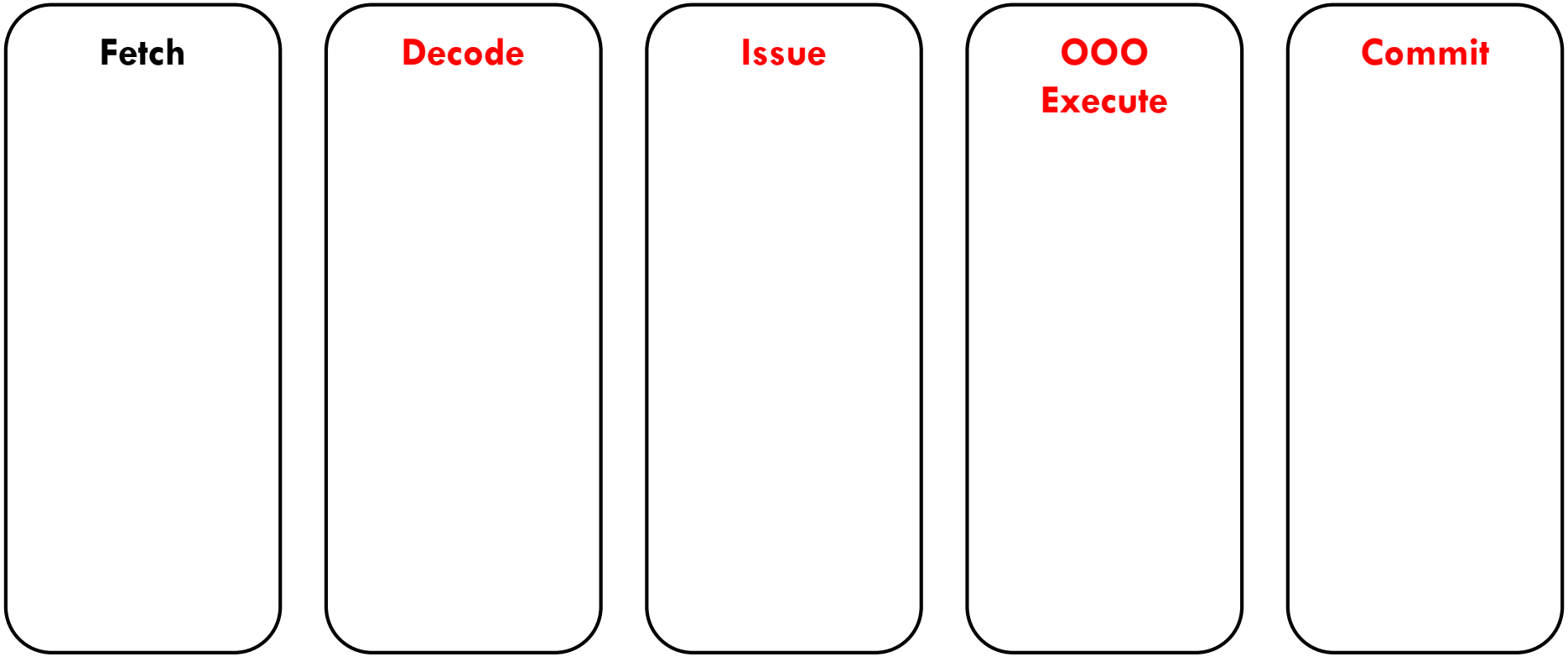

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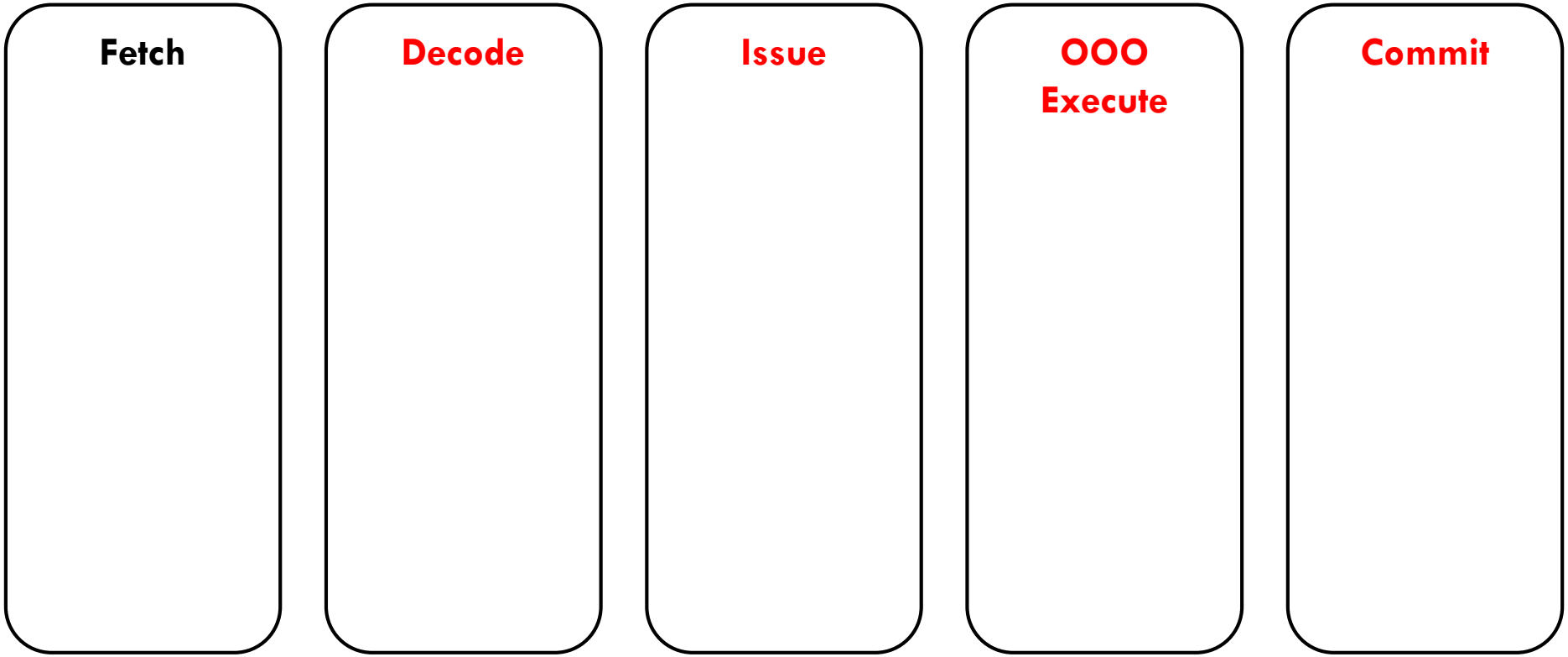

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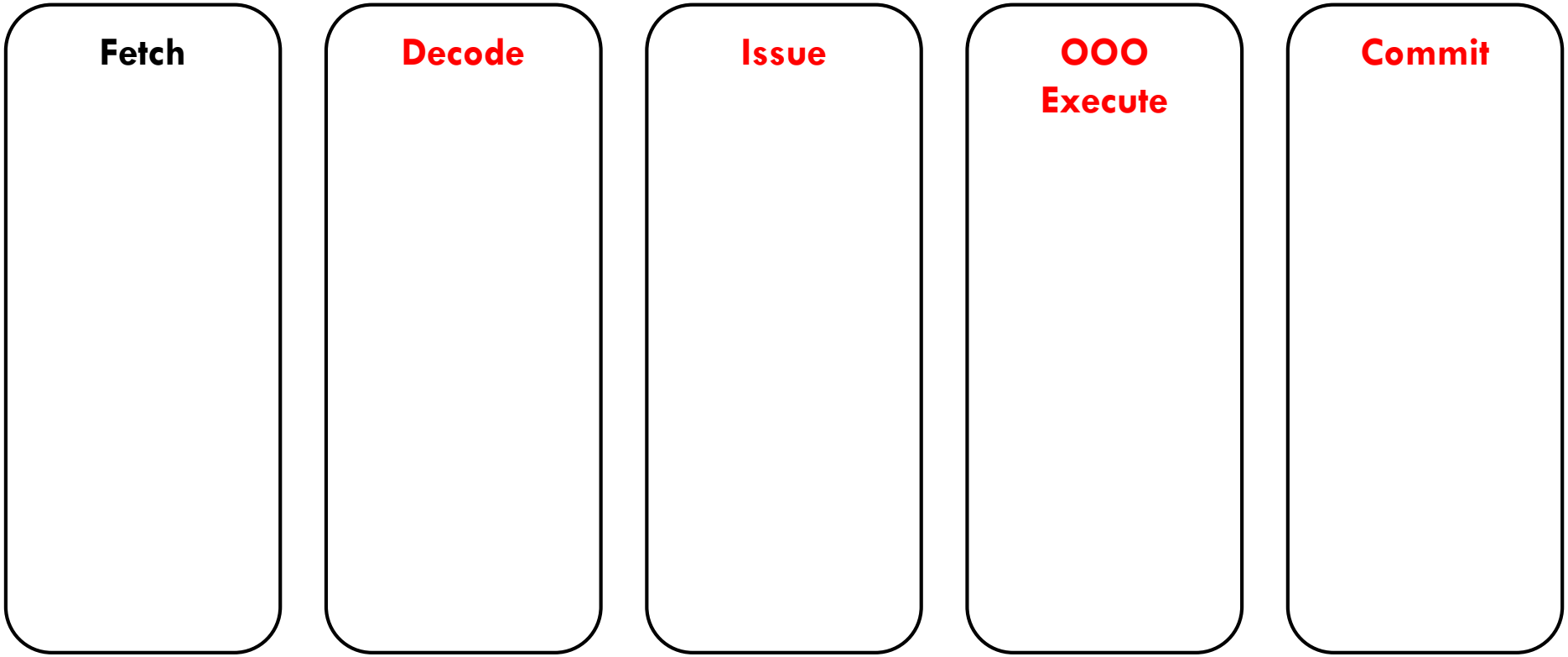

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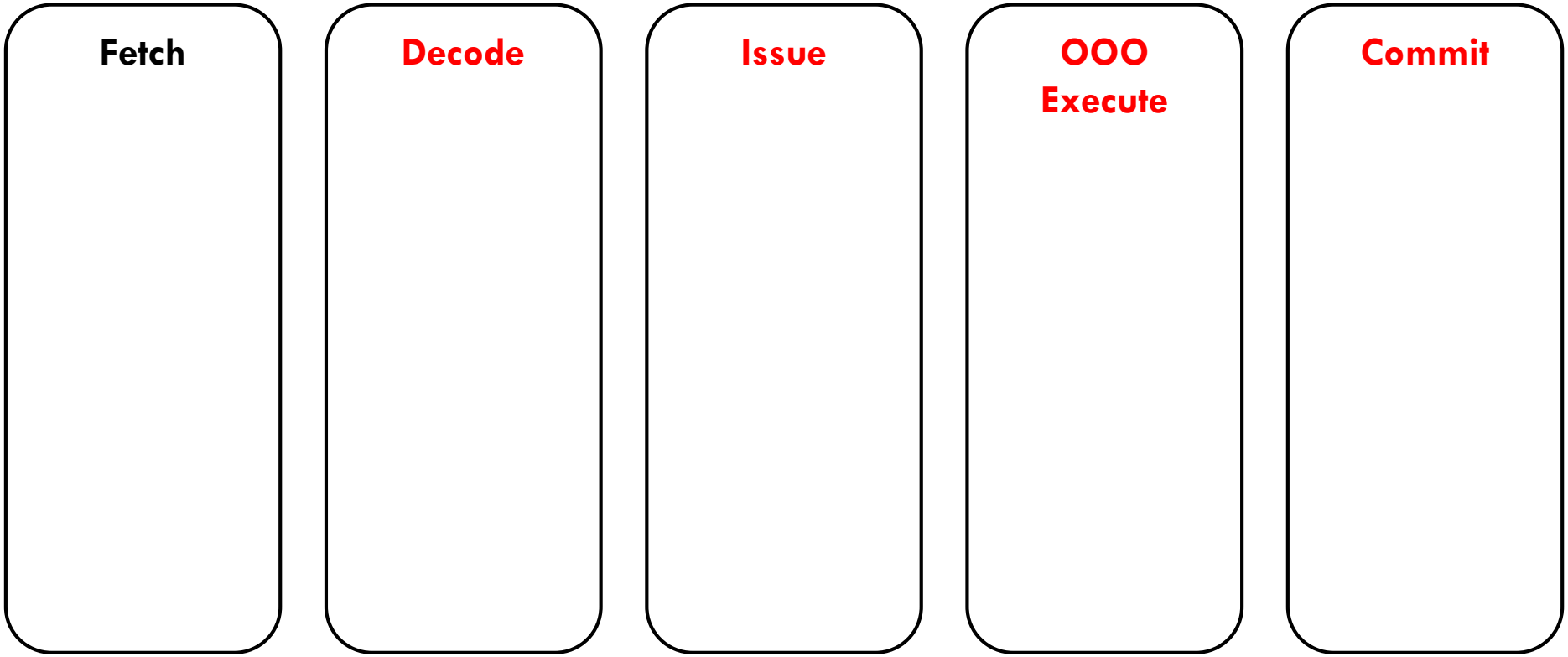

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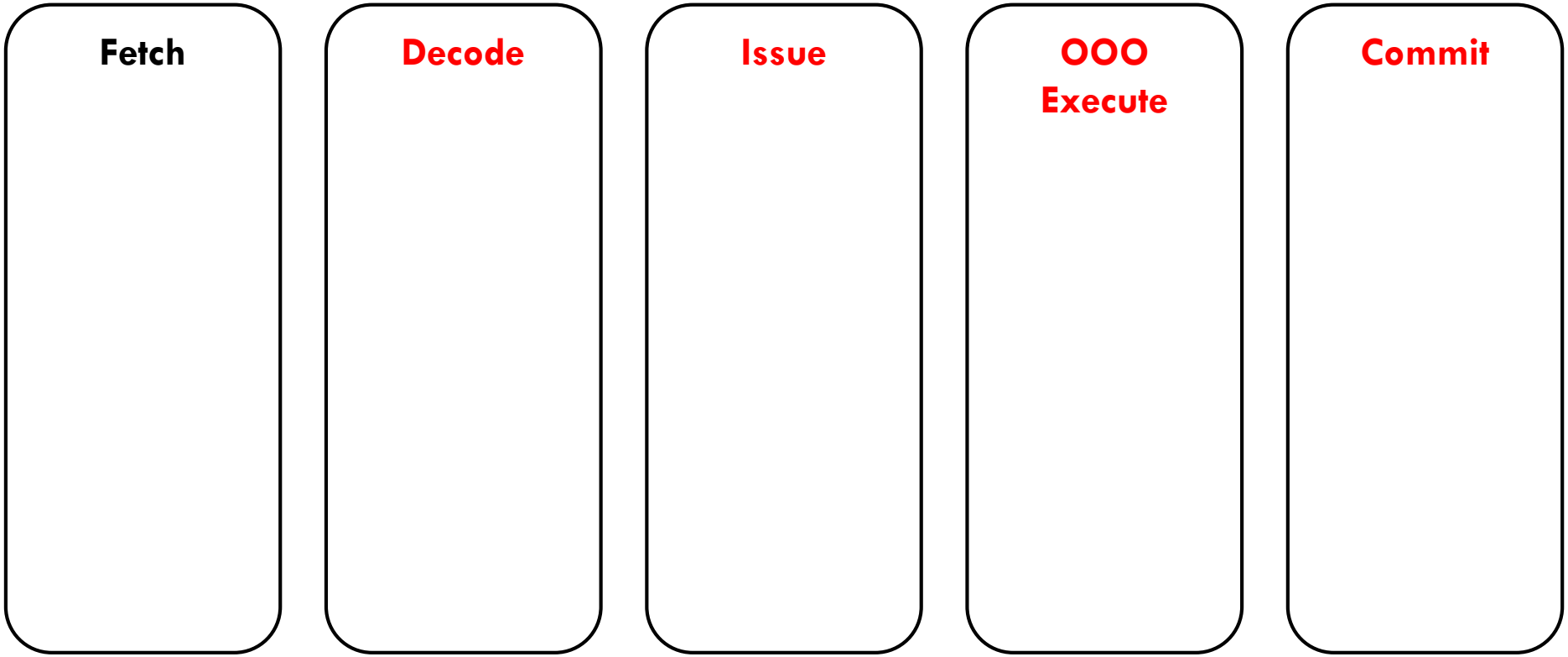

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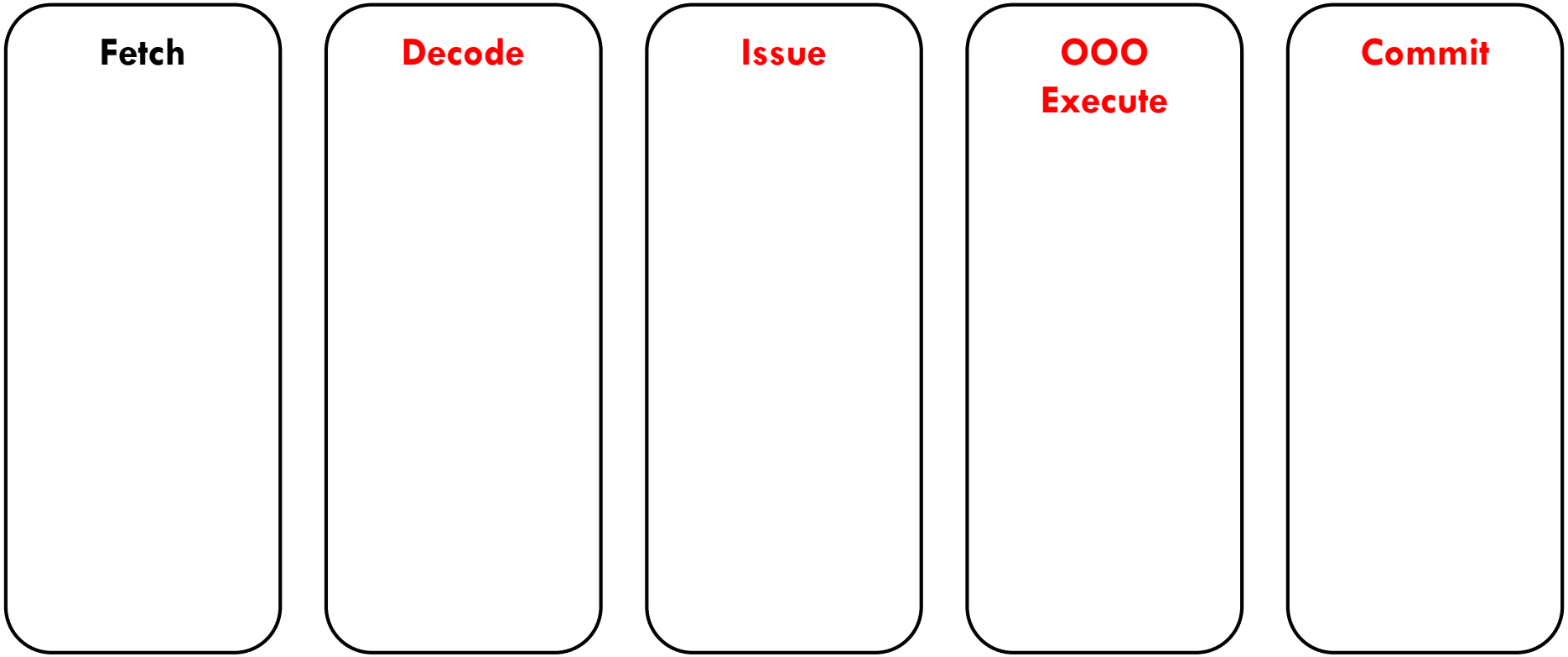

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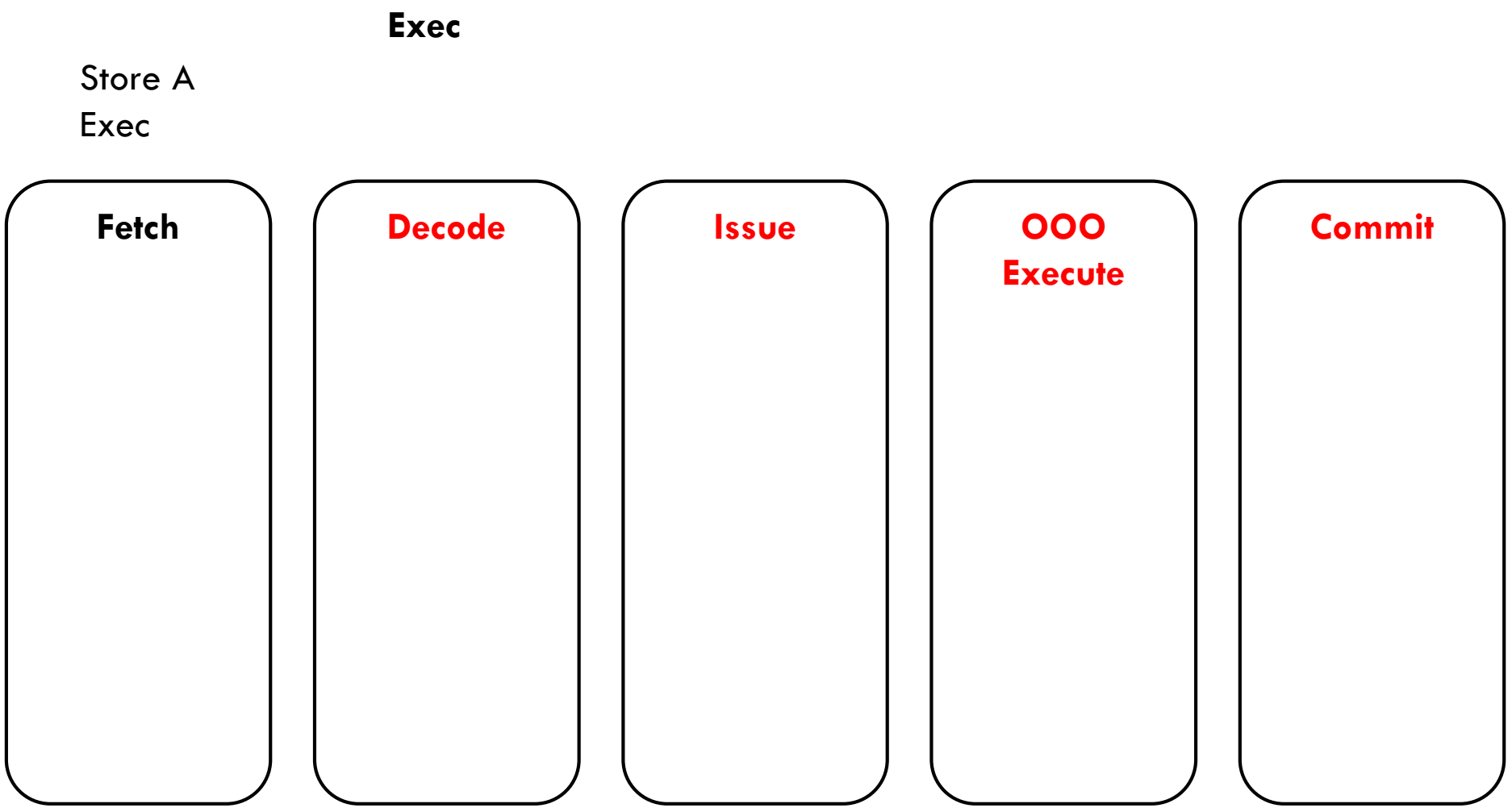

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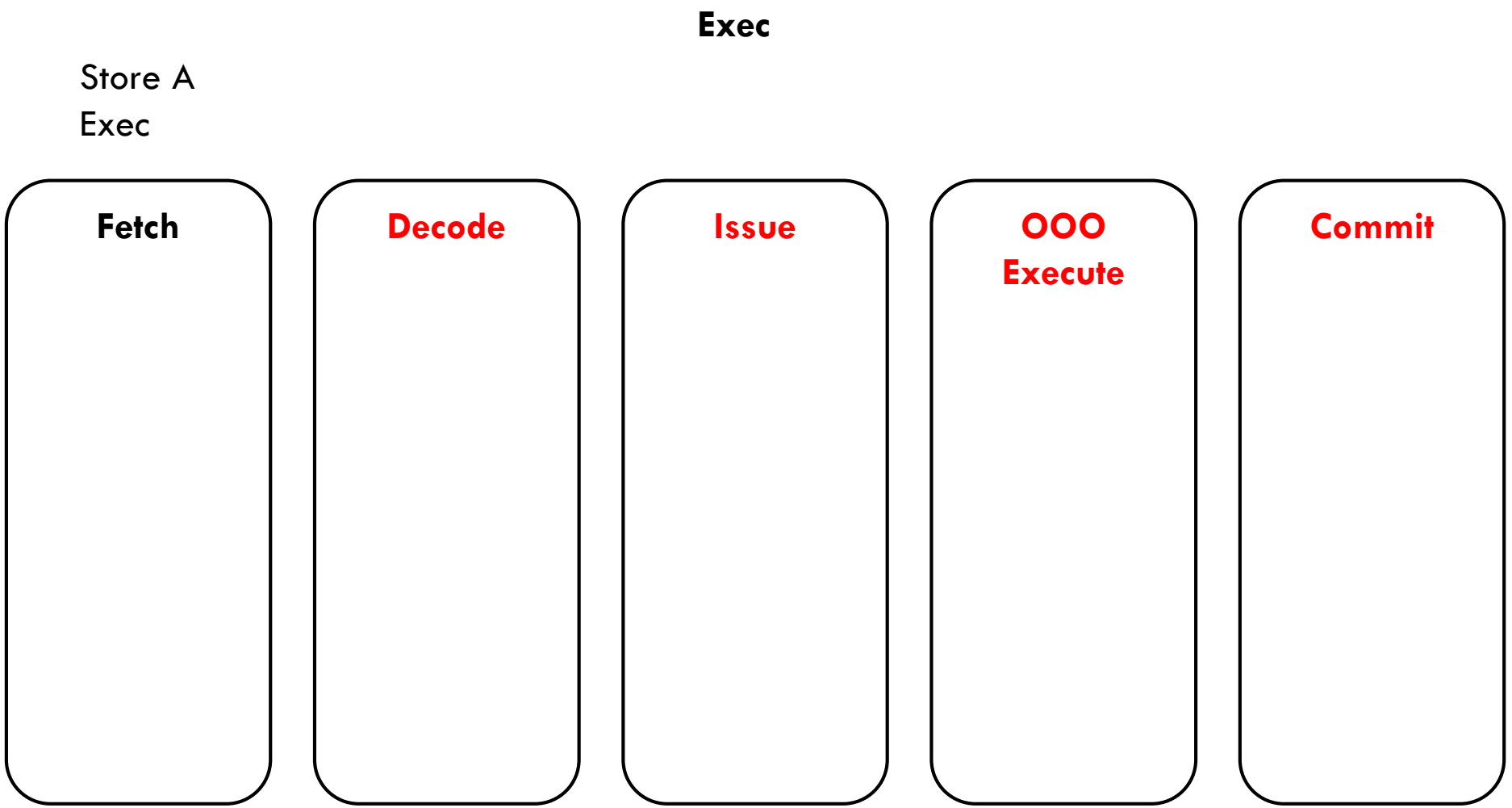

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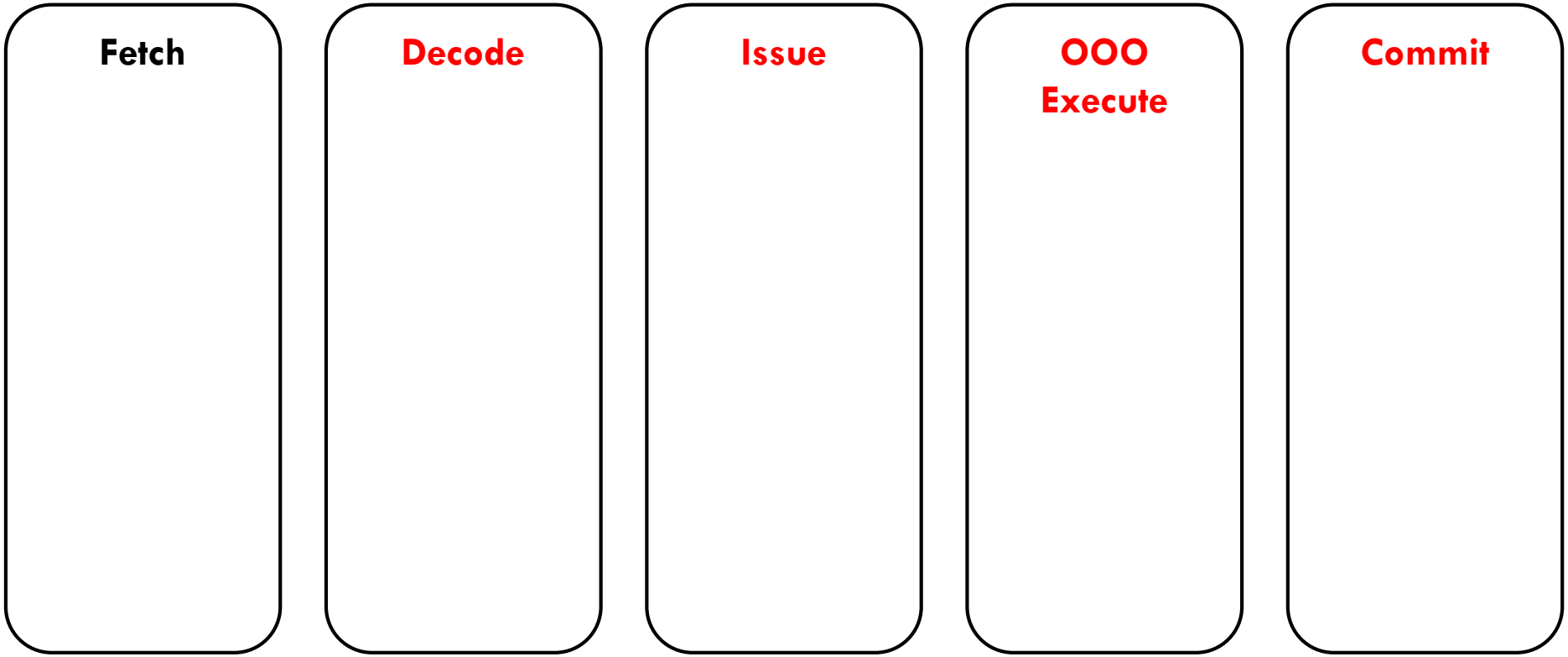

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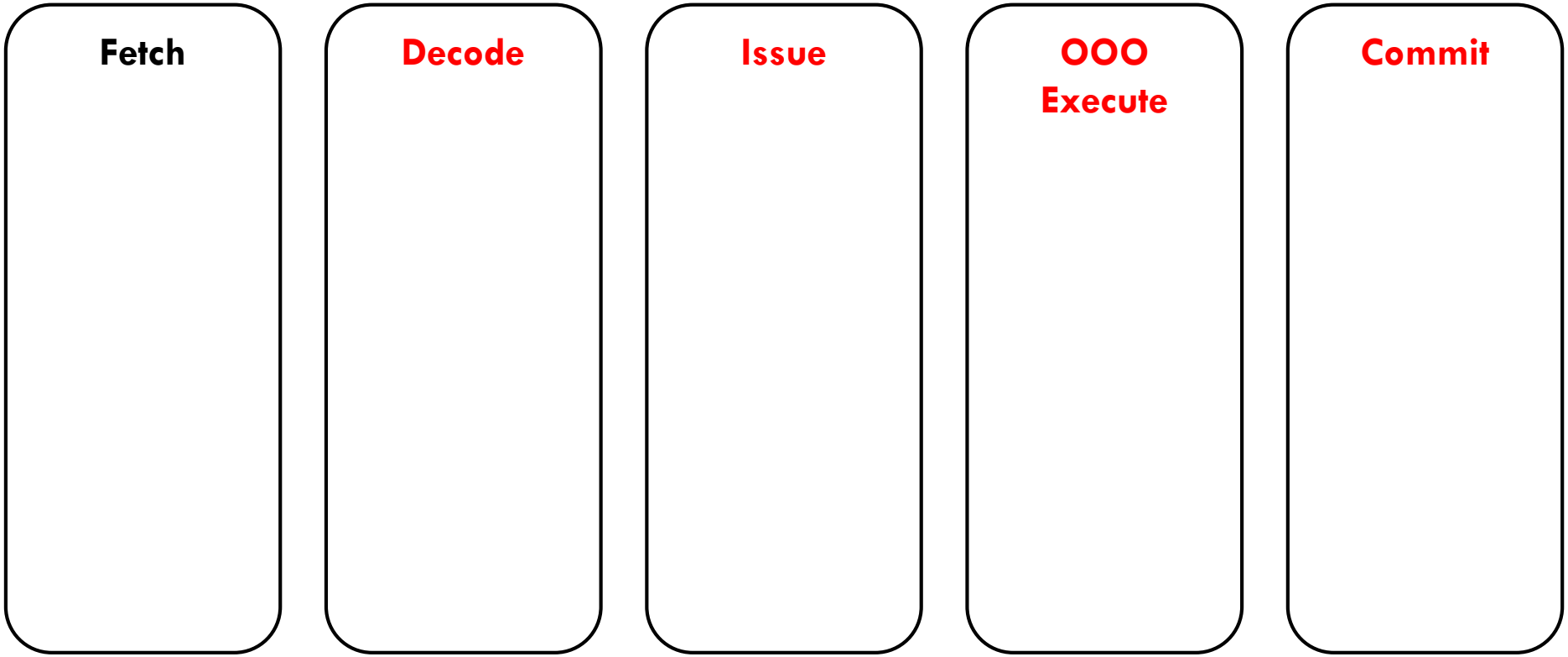

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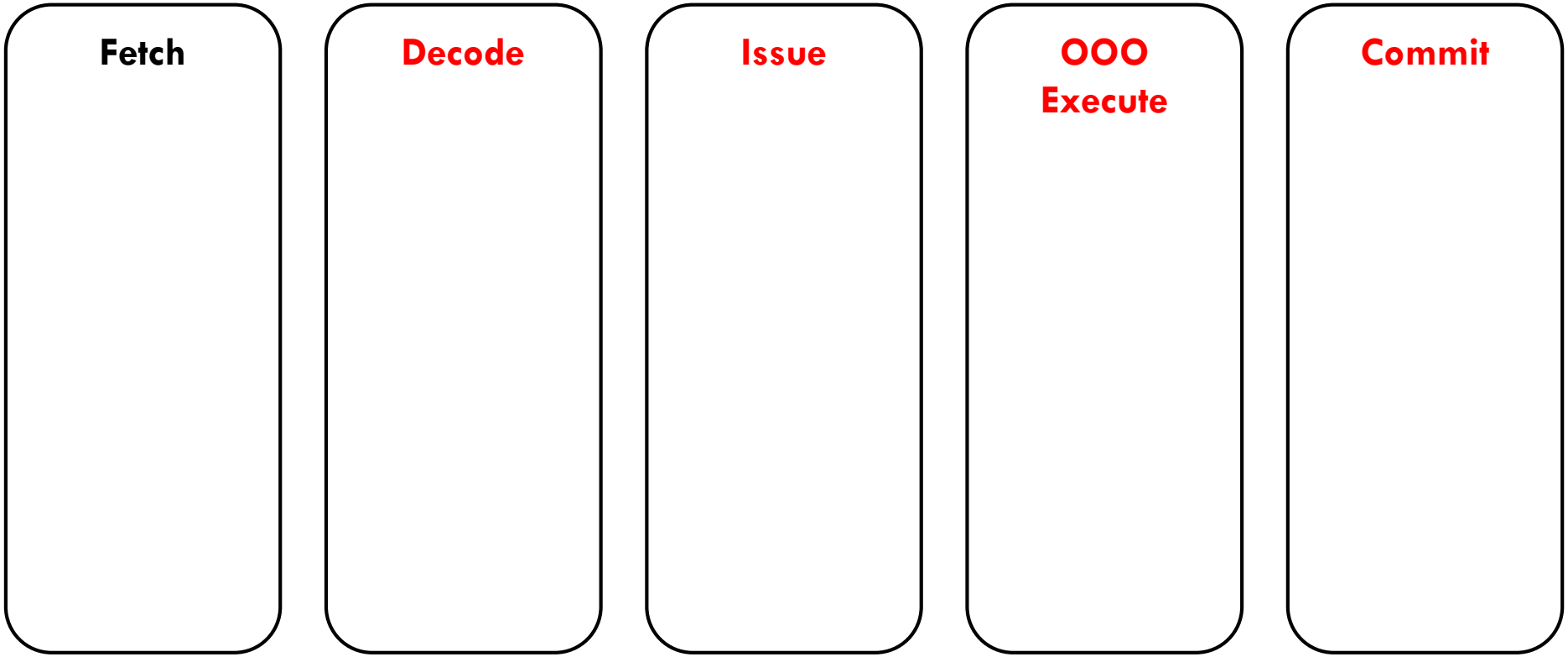

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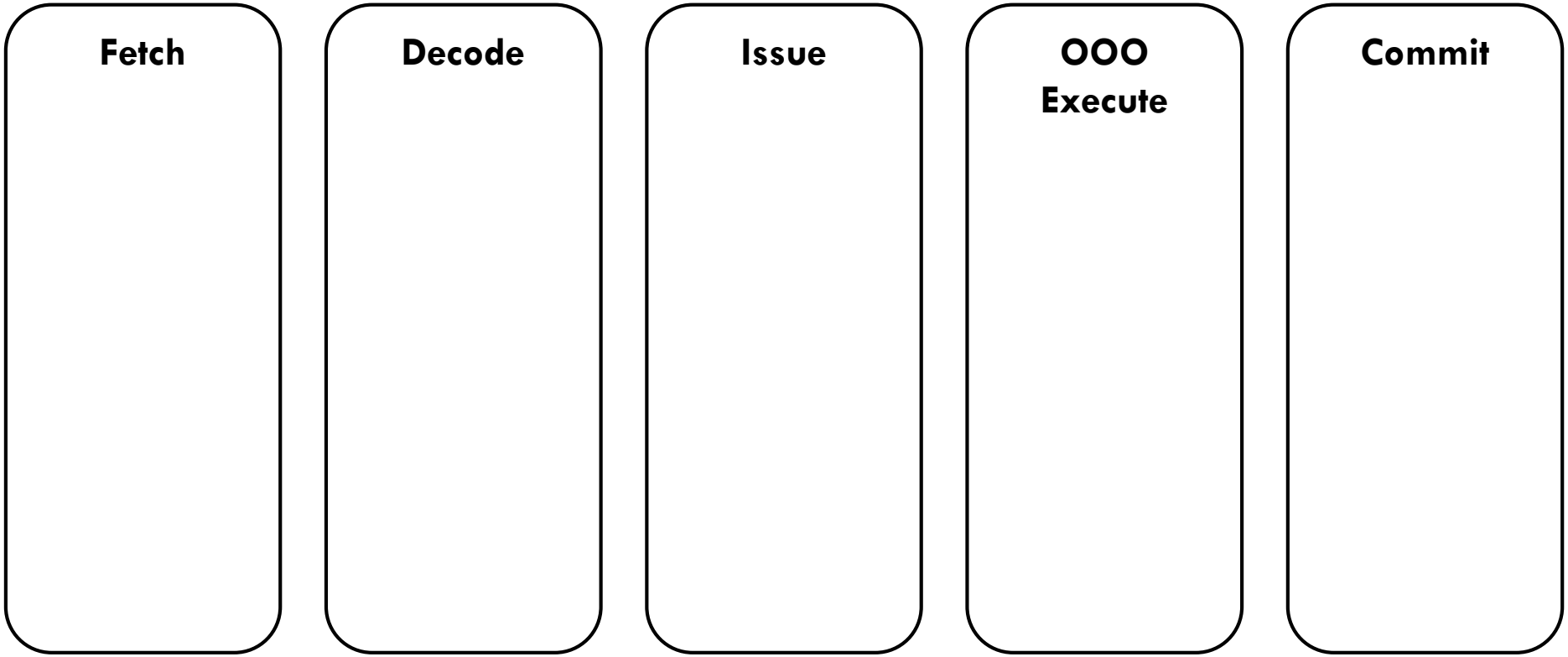

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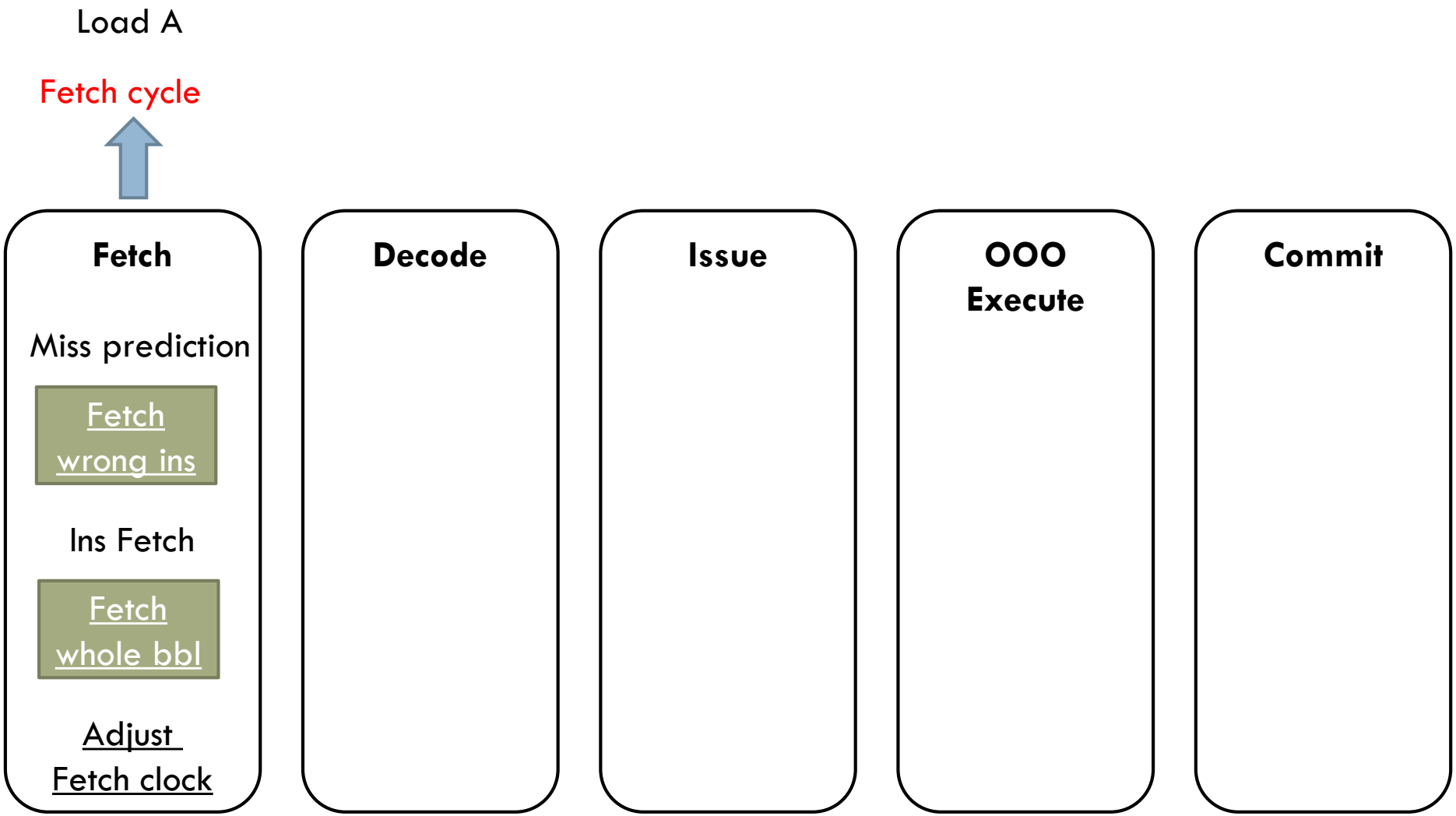

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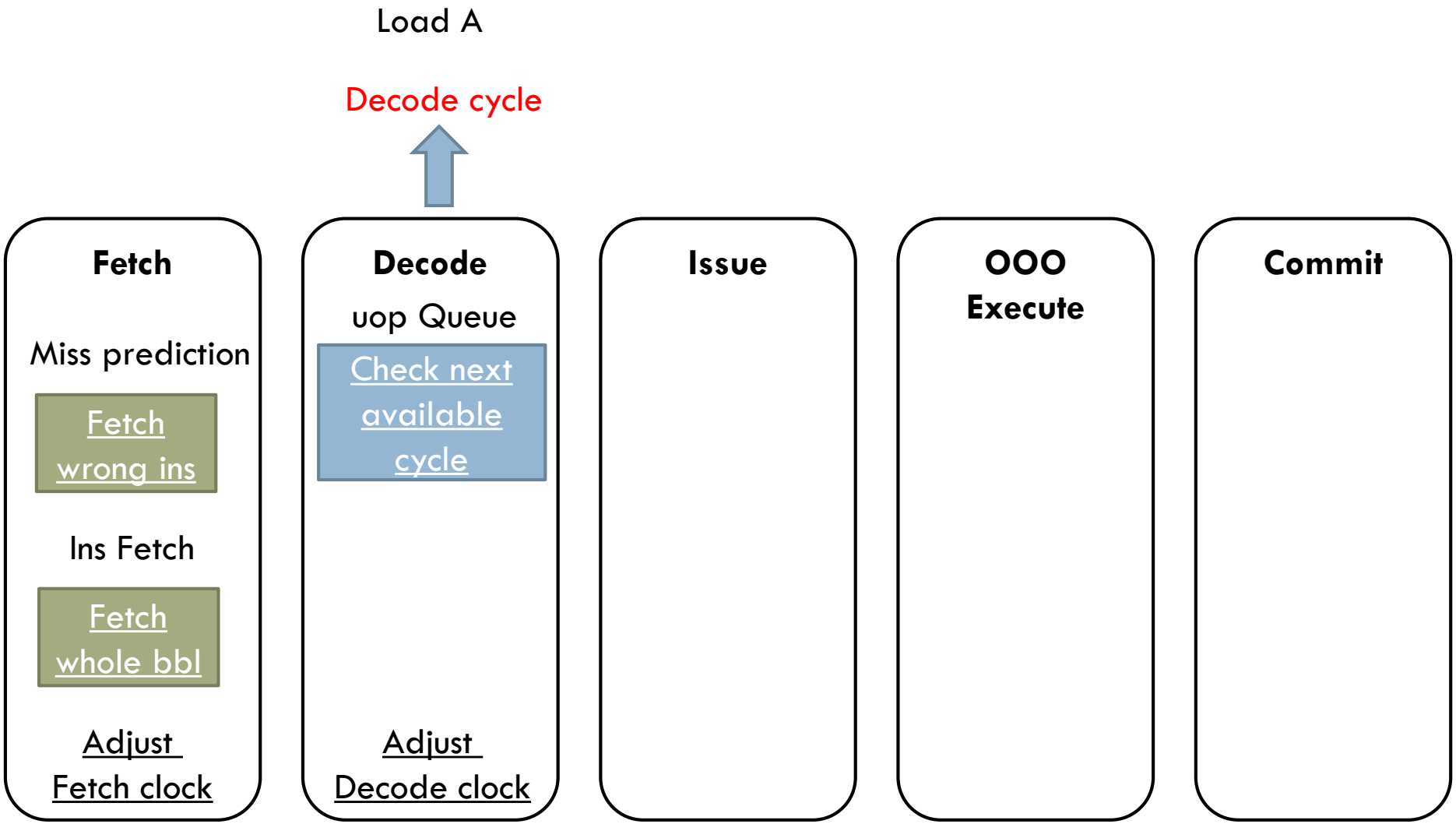

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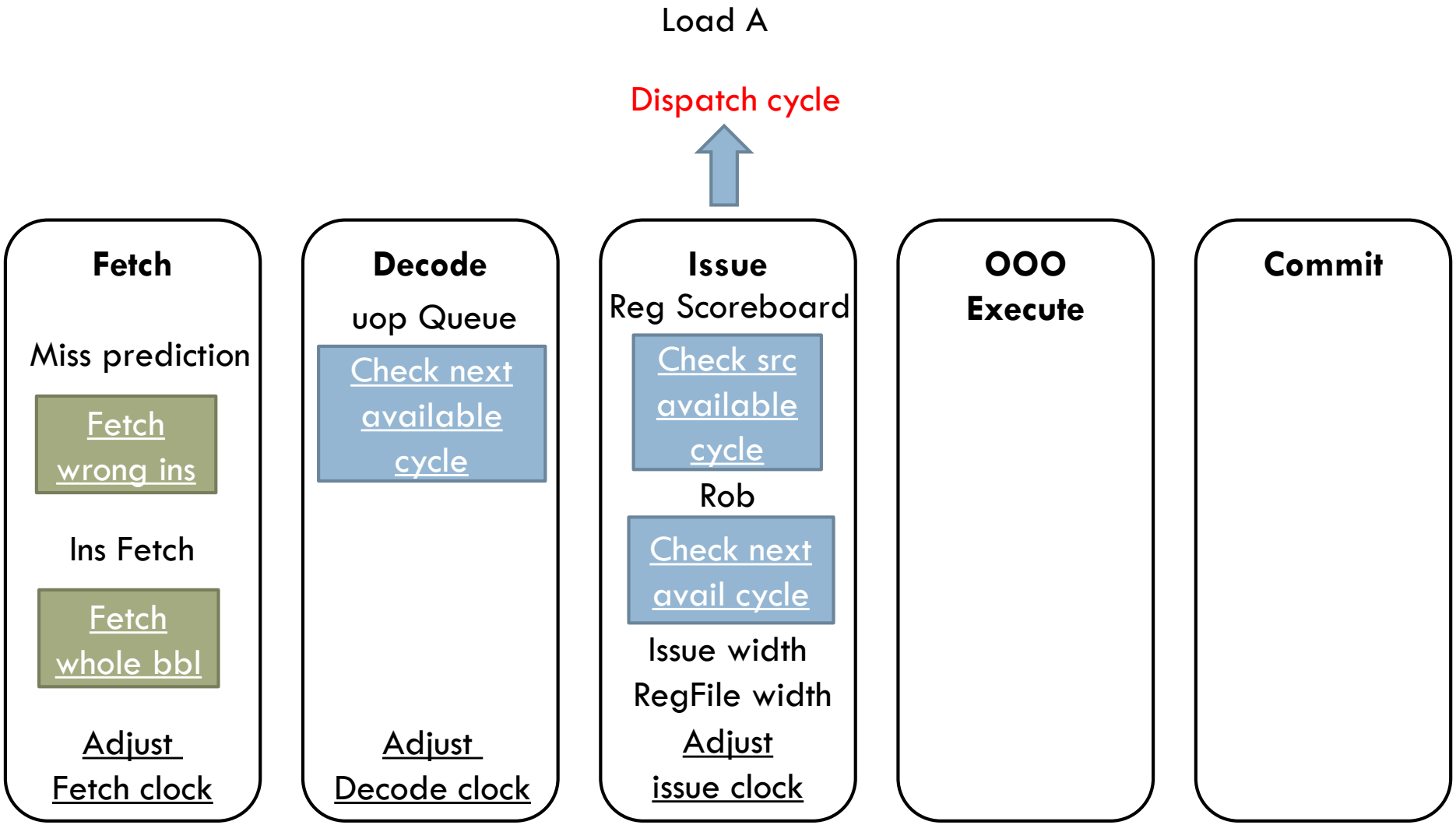

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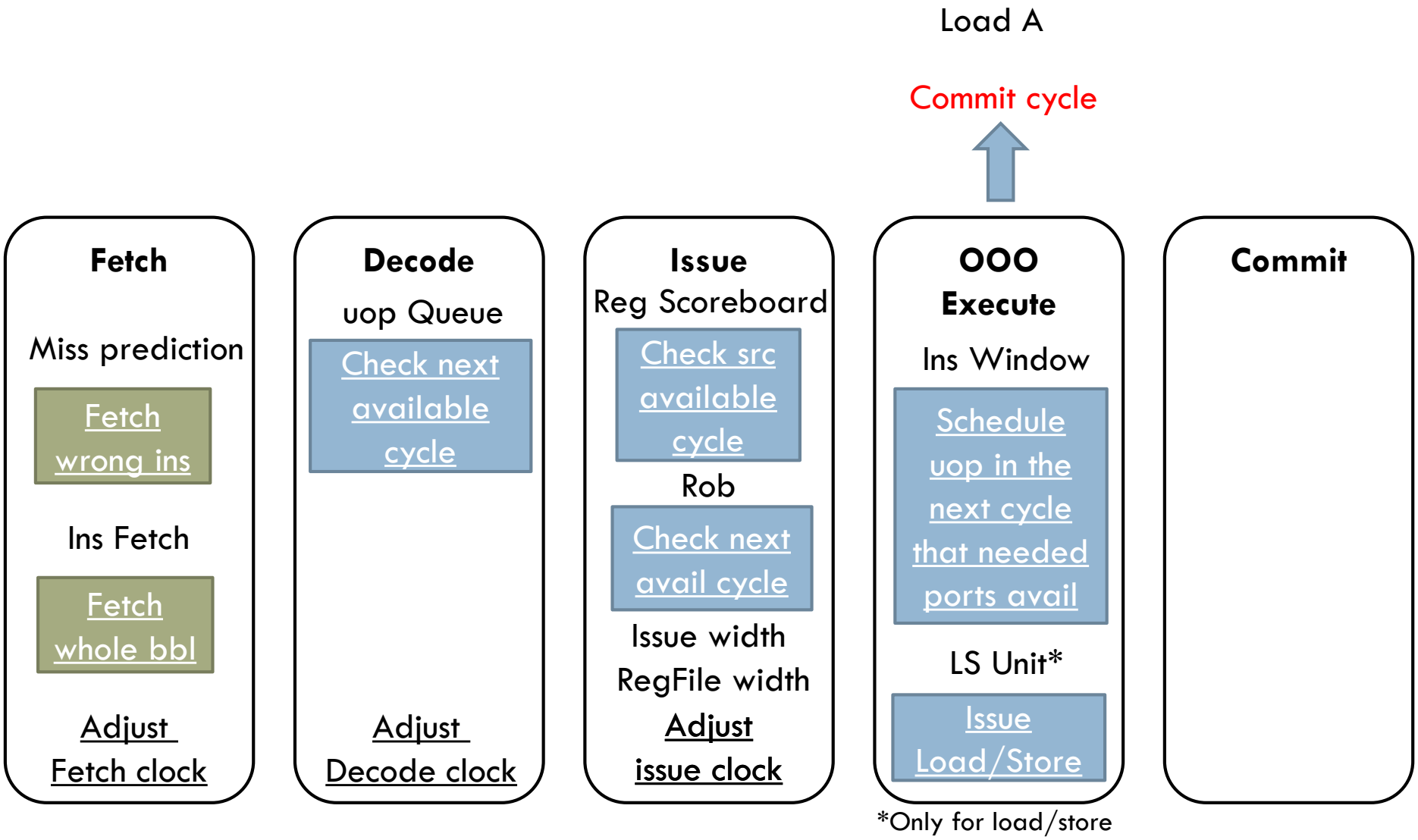

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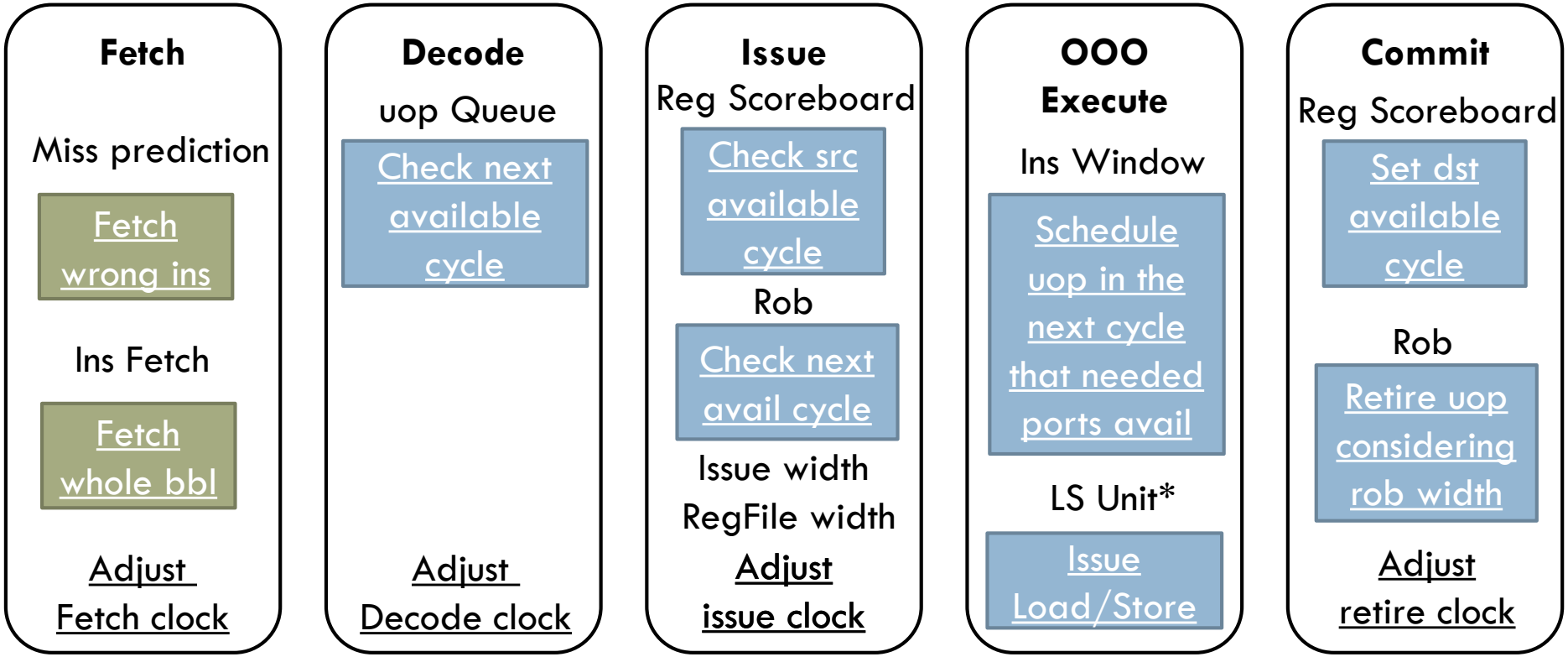

OOO Core – Load/Store

Simulate MLP

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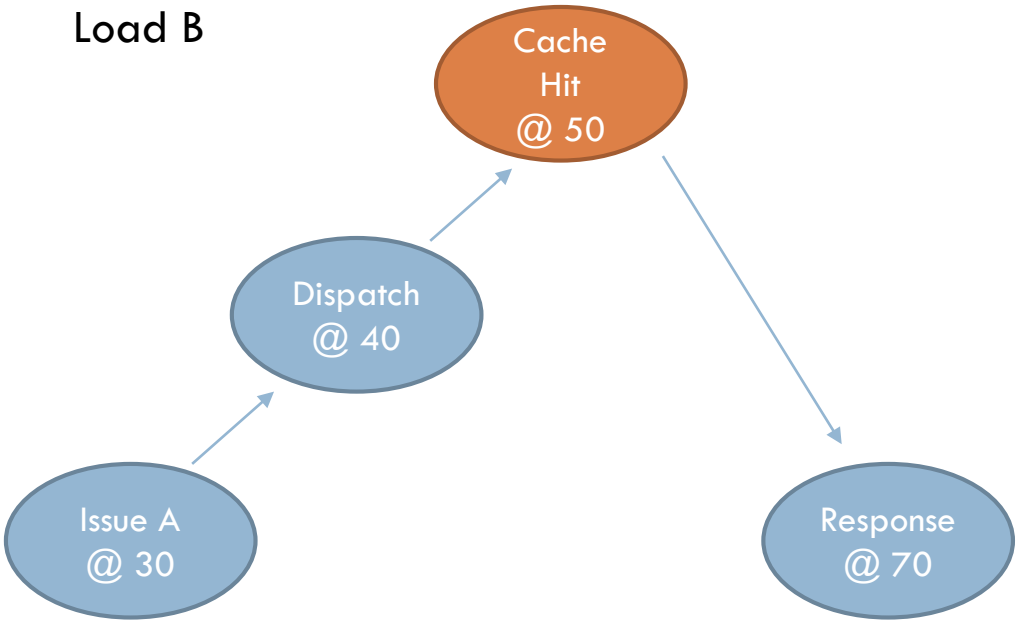

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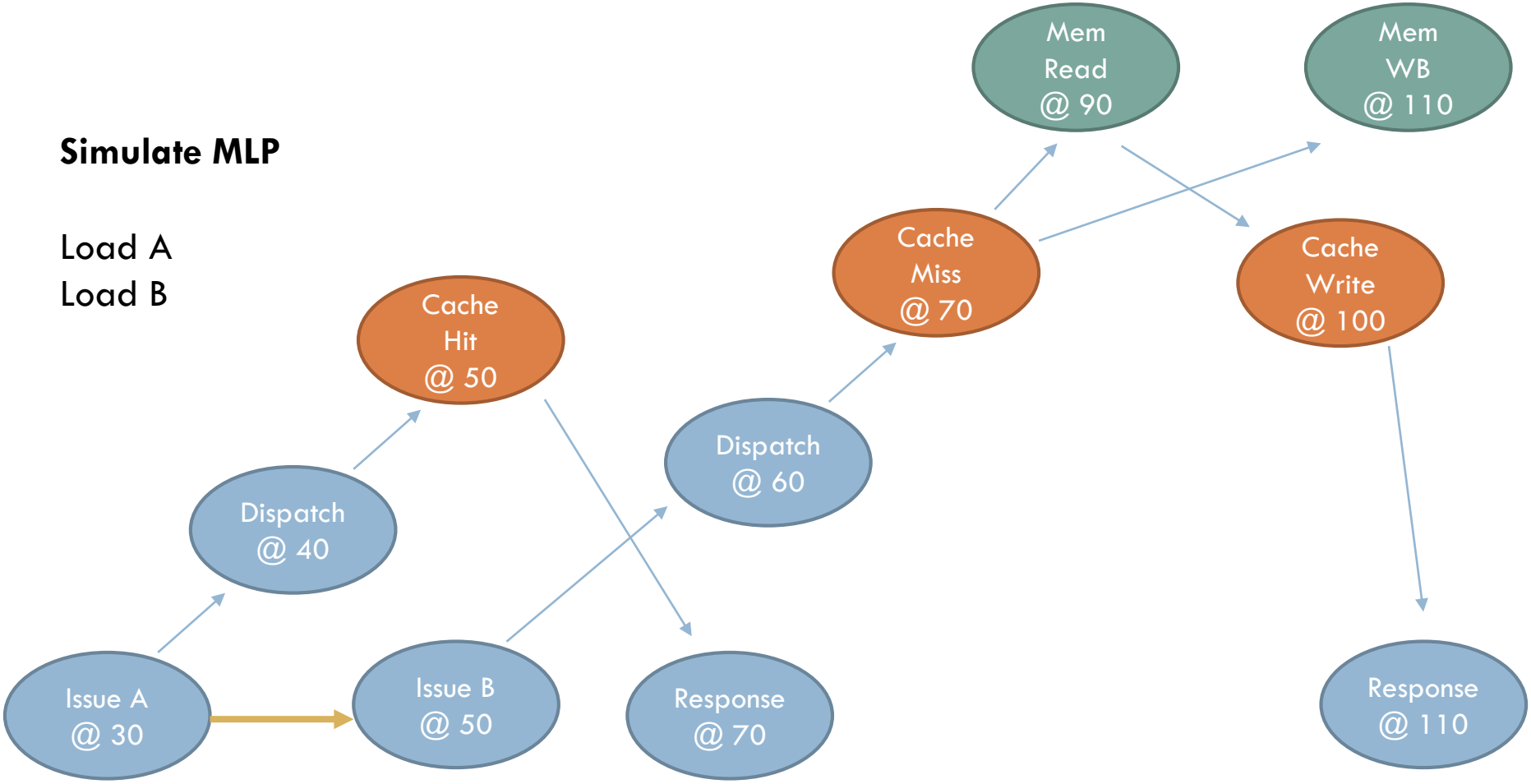

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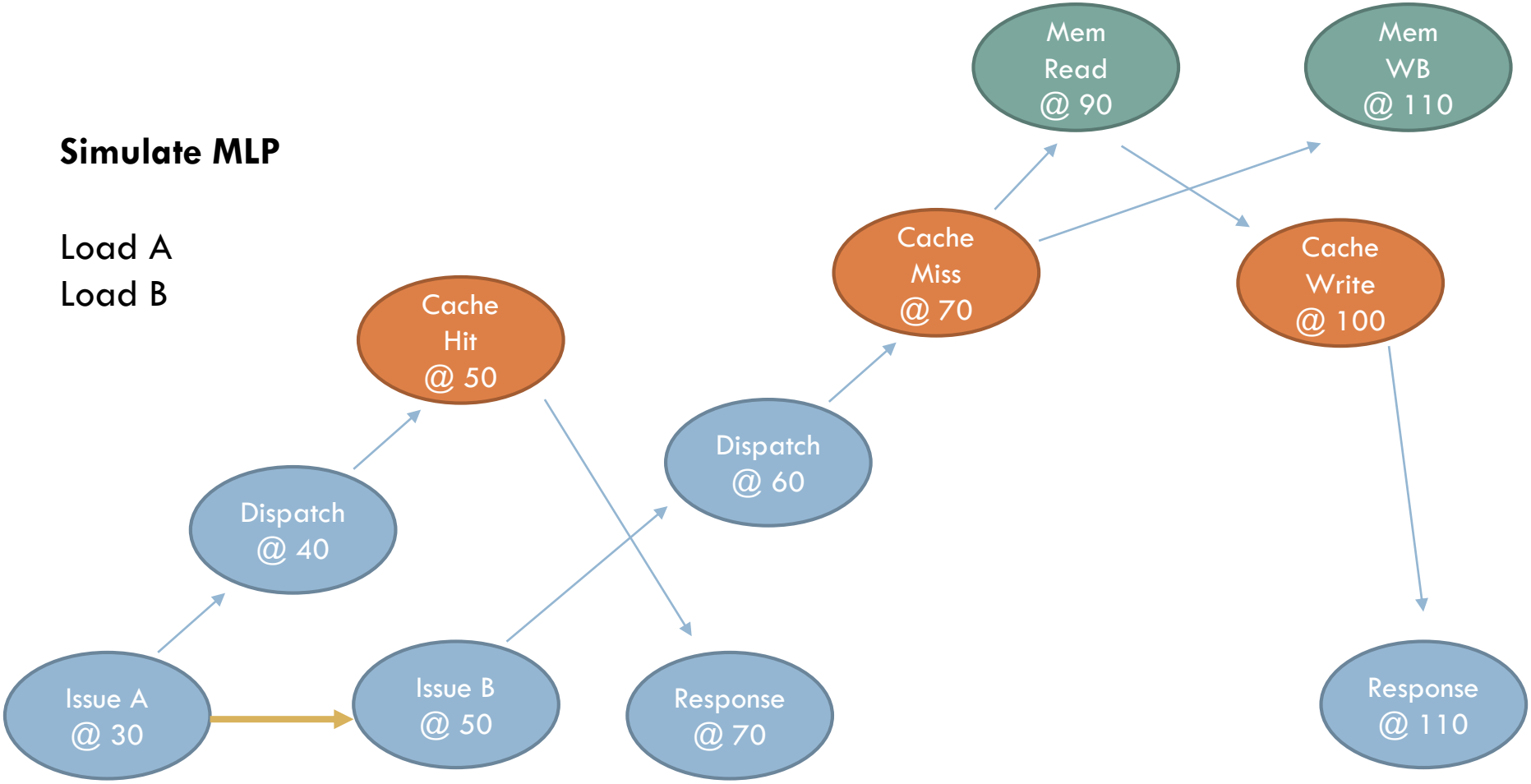
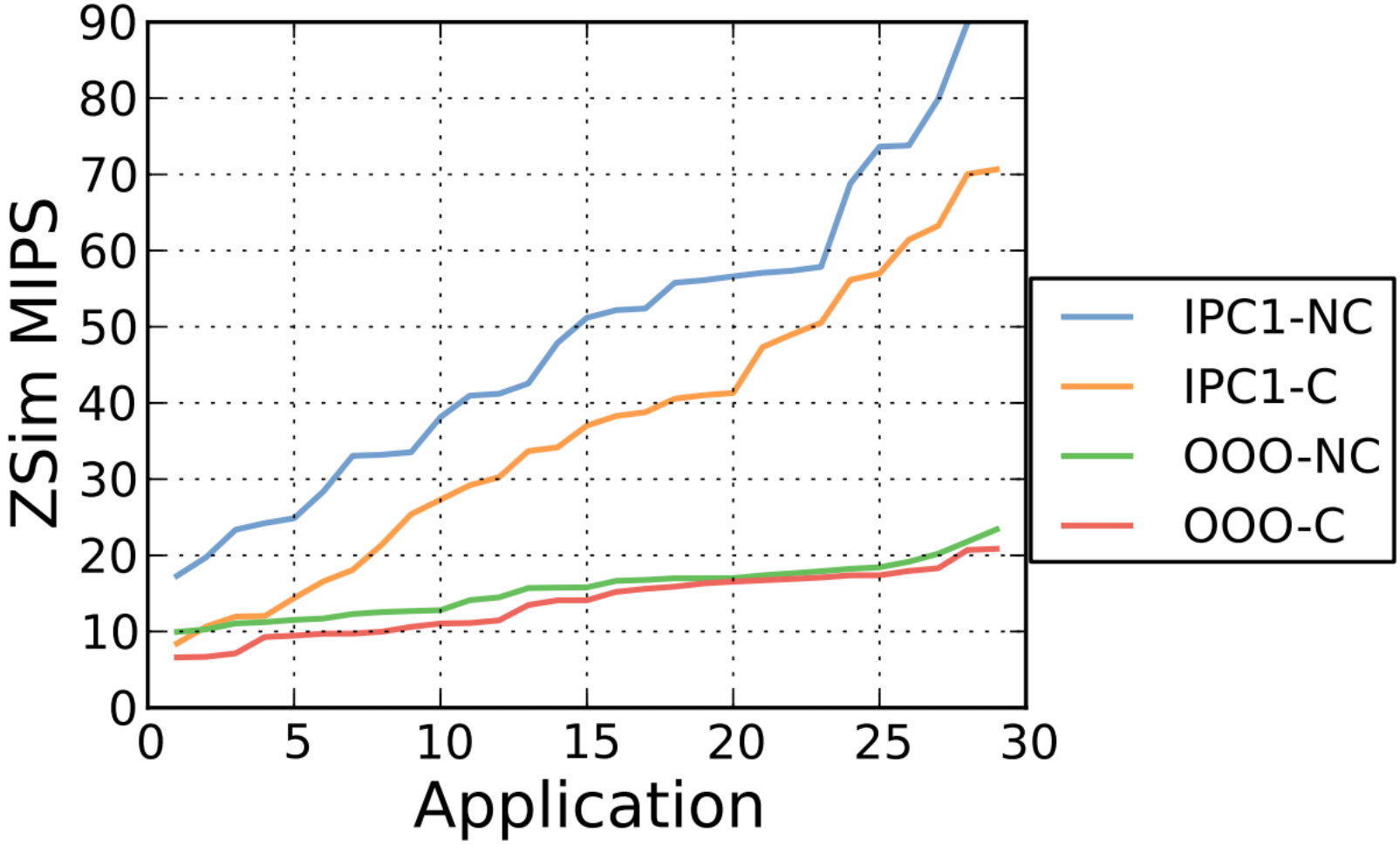


In weave phase, request B will not be delayed due to contentions for A

Simulation Speed for Different Core Type

- SPECCPU 2006 suite



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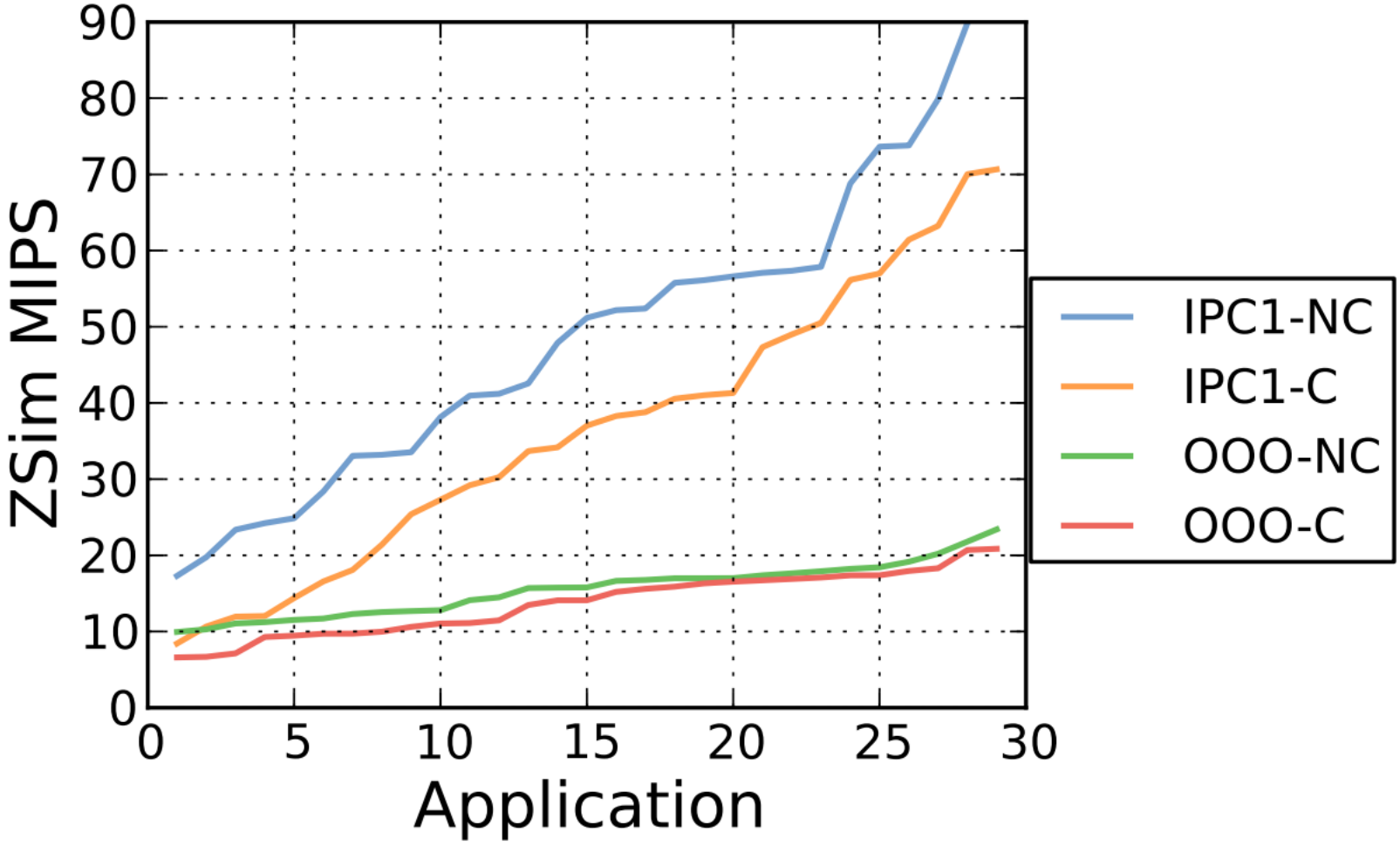
~3X difference between IPC1 and OOO-C in Hmean



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- Change OOO core type
  - From Westmere to Silvermont

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```
    //BranchPredictorPAg<11, 18, 14> branchPred;
    GSharePredictor branchPred;
```

Demo

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- Step 1: obtain the important ooo core parameters
- Step 2: change the core parameters in ooo_core.h/cpp
- Step 3: verify it against real system

Obtain Important Core Parameters

	Westmere[1]	Silvermont[2]
Issue width	4	2
F/D/I/E stages	1/4/7/13	1/3/5/8
Fetch width	16B	8B
RF read width	3	2
ROB size	128	32
Ins window	1K * 36	1K * 16
Issue queue	28	8

- [1] http://www.realworldtech.com/nehalem/
- [2] http://www.realworldtech.com/silvermont/

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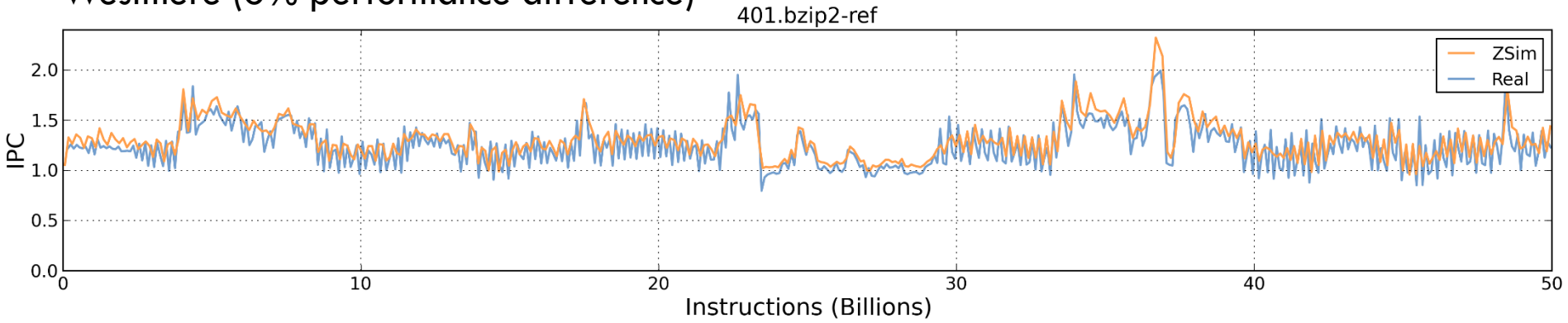
  - #define FETCH_STAGE 1 -> 1
  - #define DECODE_STAGE 4 -> 3
  - #define ISSUE_STAGE 7 -> 5
  - #define DISPATCH_STAGE 13 -> 8
  - #define FETCH_BYTES_PER_CYCLE 16 -> 8
  - #define ISSUES_PER_CYCLE 4 -> 2
  - #define RF_READS_PER_CYCLE 3 -> 2

Demo

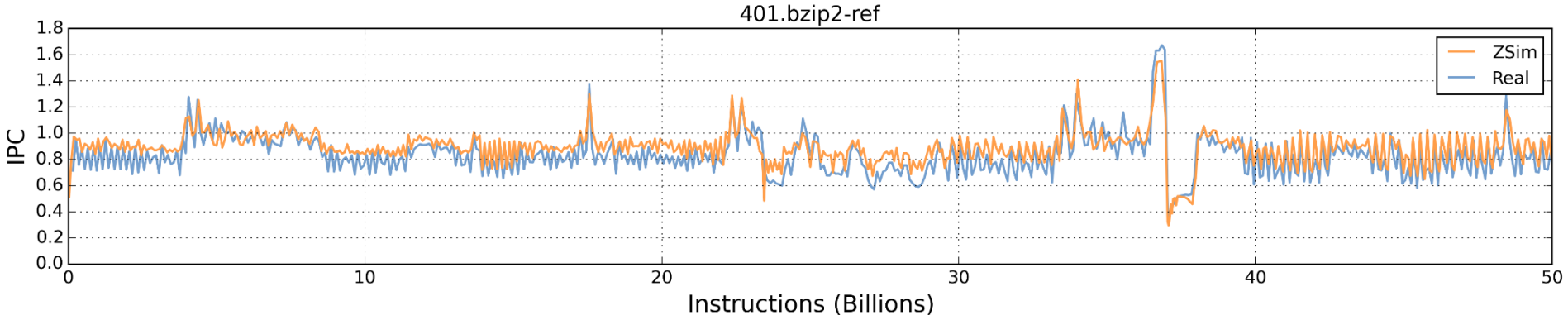
Verify It Against Real System

- IPC traces for Westmere and Silvermont

Westmere (6% performance difference)



Silvermont (9% performance difference)



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  - Westmere-like OOO core (ooo_core.h)

- Extending zsim core model is straightforward
  - Modify 4 basic analysis routines
  - Substitute the hardware structure with your implementation
  - Change the parameters in OOO

Hacking Advice

- As common Pin programming, functions in the core are very frequently called in zsim
  - You should be aware of performance when coding
  - It's the main reason why zsim statically allocates hardware structures and set ooo parameters

Thank you!

Any questions?

Break / Q&A

Try zsim now!

https://zsim.csail.mit.edu